Service Manual

Reference No. : SM- GLCT26AEADA1CS-001
Revision : 0
Date : 2007.Apr.
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In House Model No. : LCT26AE
Customer Model No. : LCT26Z4AD

BOM No : GLCT26AEADA1CS–B01

Description : Service Manual for LCT26Z4AD_CMO_USA

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0	Initial Release	2007-Apr-10

AKAI

SERVICE MANUAL

Model: LCT26Z4AD

This manual is the latest at the time of printing, and does not Include the modification which may be made after the printing, By the constant improvement of product.

Safety Precaution

CAUTION

RISK OF ELECTRIC SHOCK
DO NOT OPEN

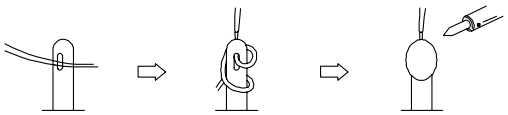
CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated “dangerous voltage” within the product’s enclo sure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements.
   Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulating Tape
   2) PVC tubing
   3) Spacers (insulating barriers)
   4) Insulating sheets for transistors
   5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.

Please leave them at an appropriate depot.

WARNING:

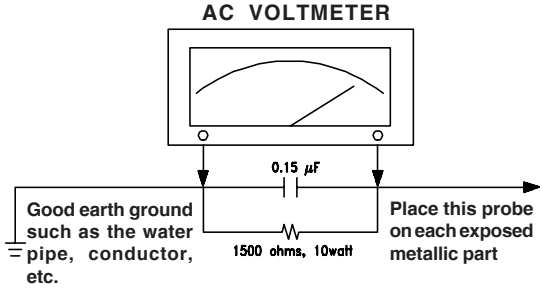
Before servicing this TV receiver, read the SAFETY INSTRUCTION and PRODUCT SAFETY NOTICE.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this apparatus. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.
4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.

5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high tempera ture components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads,metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.
   Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15μF AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.
   The measured voltage must not exceed 0.3V RMS.
   This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.
   The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.



AC Leakage Current Check

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this apparatus have special safety-related characteristics.

These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc.

The replacement parts which have these special safety characteristics are identified by ⚠ marks on the schematic diagram and on the parts list.

Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, or other hazards.

9. Must be sure that the ground wire of the AC inlet is connected with the ground of the apparatus properly.

Technical Specification

Product Model	LCT26Z4AD
TV System	NTSC M, ATSC
VIDEO System	NTSC
Screen Size	26” diagonal
Active Area	575.8mm(H) x 323.7mm(V)
Aspect Ratio	16:9
External Size (with stand)	715.43 mm (W) x 554.62 mm (H) x 115.07 mm (D)
Gross Weight (with stand)	17.3 kg
Display Resolution	1366 (H) x 768 (V) pixels (Each pixel has R/G/B 3 color cells)
Pixel Pitch (Sub Pixel)	0.1405 (H) x 0.4215 (V) mm
Display Color	16.2 millions of colors (R/G/B each 256 scales)
Gray Scale	256 (R/G/B each 8-bit)
Brightness (Peak Value)	500cd/m^2
Contrast (Dark Room)	800:1
Sound Effect	Acoustic Cinema Enhancement
Power Supply	AC 120V, 60 Hz
Power Consumption	160W
Input Terminal	Antenna Input (F Type) x 1 (NTSC + ATSC/Clear QAM)
	HDMI (Ver1.2) connector x2
	VGA (D-Sub 15 Pin Type) x 1
	Component Video - YPbPr x 1 RCA Terminals
	Video Input RCA Terminals x 1
	S-Video Input Mini Din 4 Pin Terminal x 1
	Stereo, Audio x 4
Output Terminal	1 set of Audio Output terminals (RCA, L&R)
	SPDIF (Coaxial for all) x 1
	SPDIF (Coaxial only for DVD) x 1

Note: The specifications shown above may be changed without notice for quality improvement.

Support the Signal Mode

A. VGA Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
640 x 480	31.50	60.00
800 x 600	35.16	56.25
	37.90	60.32
	48.08	72.19
1024 x 768	48.40	60.00

B. YPbPr Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480p(720x480)	31.468	59.94
720p(1280x720)	45.00	60.00
1080i(1920x1080)	33.75	60.00

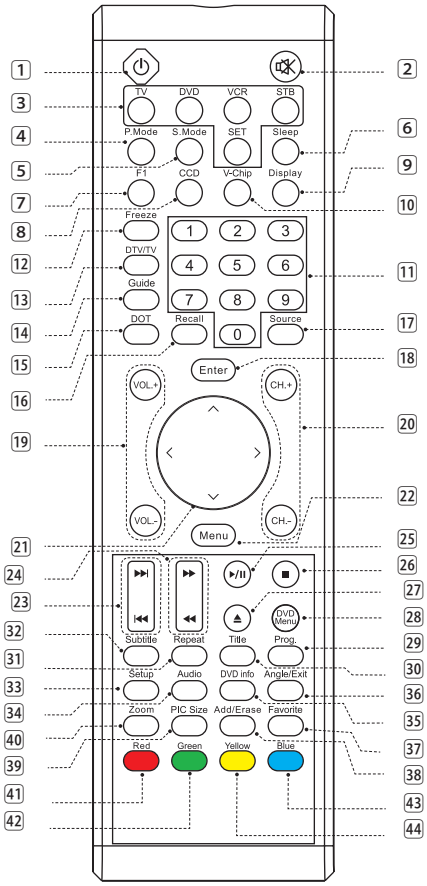
C. HDMI Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480p	31.468	59.94
720p	45.00	60.00
1080i	33.75	60.00

- When the signal received by the Display exceeds the allowed range, a warning message shall appear on the screen.
- You can confirm the input signal format from the on-screen.

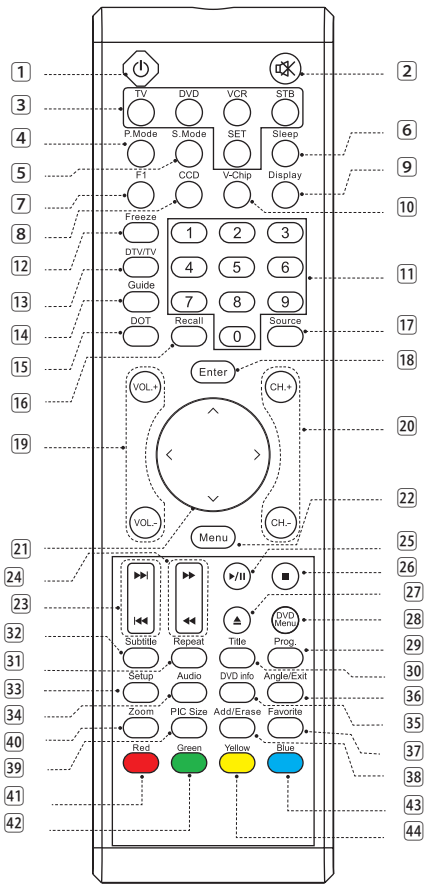
Remote Control

(Note: *Details refer to AKAI TV Universal Remote Control Programming & Codes Guide.)*



1 **Standby(⏻):** Press to turn on and off.
2 **Mute(🔇):** Press this button to quiet the sound. Press again to reactivate the sound.
3 Press these buttons to select control of the TV, DVD, VCR or Set-top Box device.
4 **P. Mode**: Press to cycle through the picture modes: Cinema, Normal, Vivid, Hi-Bright and User.
5 **S. Mode**: Press to cycle through the sound modes: Normal, News, Cinema, Concert and User.
6 **Sleep**: Press repeatedly until it displays the time in minutes (10, 20, 30, 40, 50, 60, 90, 120 and Off) that you want the TV to remain on before shutting off. To cancel sleep time, press **Sleep** button repeatedly until sleep Off appears.
7 **F1**: Press to cycle through the Stereo and Multi-channel TV sound options: Mono, Stereo and Bilingual.
8 **CCD**: Press to select the Closed Caption mode.
9 **Display**: Press to display the channel information;this information disappears after 9 seconds.
10 **V-Chip**: Select the child protect mode you want.
11 **0~9 Number Buttons**: Press 0~9 to select a channel, and input the password
12 **Freeze**: This button does not function on your TV LCT26Z4AD since it does not have “freeze” feature.
13 **DTV/TV**: Press to choose DTV/TV (high definition channels) directly.
14 **Guide (Digital TV Timetable)**: Press to display the (Digital TV Timetable) mode. Press again to exit.
15 **DOT:** Press number buttons with it to select the channels directly in DTV.(i.e. channel 108-1 would need the dot button after the 8)
16 **Recall**: Press to return to previous channel. (Only for TV)
17 **Source**: Press to select the signal source, such as TV, AV, S-Video, YPbPr, DVD, VGA, HDMI 1 or HDMI 2.
18 **Enter**: Press to enter or confirm.
19 **VOL +/-**: Press to adjust the aduio levels.
20 **CH +/-** : Press to select the channel forward or backward.
21 ∧, ∨, <, >: Press ∧, ∨, <, > to move the on-screen cursor.
22 **Menu**: Press to enter into the on-screen setup menu, press again to exit.
23 ⏮, ⏭ : Press to skip the backward or forward.
24 ◀◀, ▶▶ : Press to search the backward or forward.
25 ▶/⏸ : Press to play or pause the DVD disc.
26 ■ : Press to stop playing the disc.
27 ⏏ : Press to stop playing the disc.
28 **DVD Menu**: Press to return DVD disc menu.
29 **Prog.**: Press to display the program menu. Press it again to exit.
30 **Title**: Press to display to DVD disc title.

31 **Repeat**: When in DVD mode, press to cycle through the options: CHAPTER, TITLE, ALL and nothing. While in CD mode, the options are: TRACK, ALL.
32 **Subtitle**: Press to select desired DVD subtitle.
33 **Setup**: Press to display a setup page. Press it again to exit menu.
34 **Audio**: Press to select desired audio track.
35 **DVD Info**: Press to display DVD information.
36 **Angle/Exit**: Press this button to select desired viewing angle of the Video (disc feature).
37 **Favorite**: Press to select the favorite channel from list.
38 **Add/Erase**: Press to add or delete favorite channels.
39 **Pic Size**: Press to change the screen size, such as Full, 4:3.(Note: When in VGA mode, it can only select “Full”.)
40 **Zoom:** This button is not in use.
41 **Red**: This is a special control function for the Digital tuner.
42 **Green**: This is a special control function for the Digital tuner.
43 **Yellow**: This is a special control function for the Digital tuner.
44 **Blue**: This is a special control function for the Digital tuner.



DTVS205CH201A
Digital/Analog
Tuner

MT5112BD
DTV Demodulator

LCD panel

POWER BOARD

5V
Standby 5V
12V
9V
24VA (For Class D)

CVBS/SIF

10Bit LVDS

TS Dock

MAIN BOARD

HDMI1
HDMI2

Two to one
HDMI Switch

TMDS

Coaxial
Output

COAXIAL

24C16
EEPROM

Flash
32M

NJRC4558
Audio Buffer

Audio
Output

DDR
256M

Comp
DVD
VGA
AV
S-Video

MT5370
ADC
Scaler
ATSC
LVDS Transfer

IIS

Audio
X4

CE2836
Audio
ADC&DAC

Max232
Level Shift

RS232
Socket

R2S15102
Class D
Amplifier

Relay

Speaker

COMB DVD

Am5888
SL/F
Motor
Driver

Loader
&Optical
Pick up

To HET-4052

4334KSZ
Audio DAC

ToQS3VH257

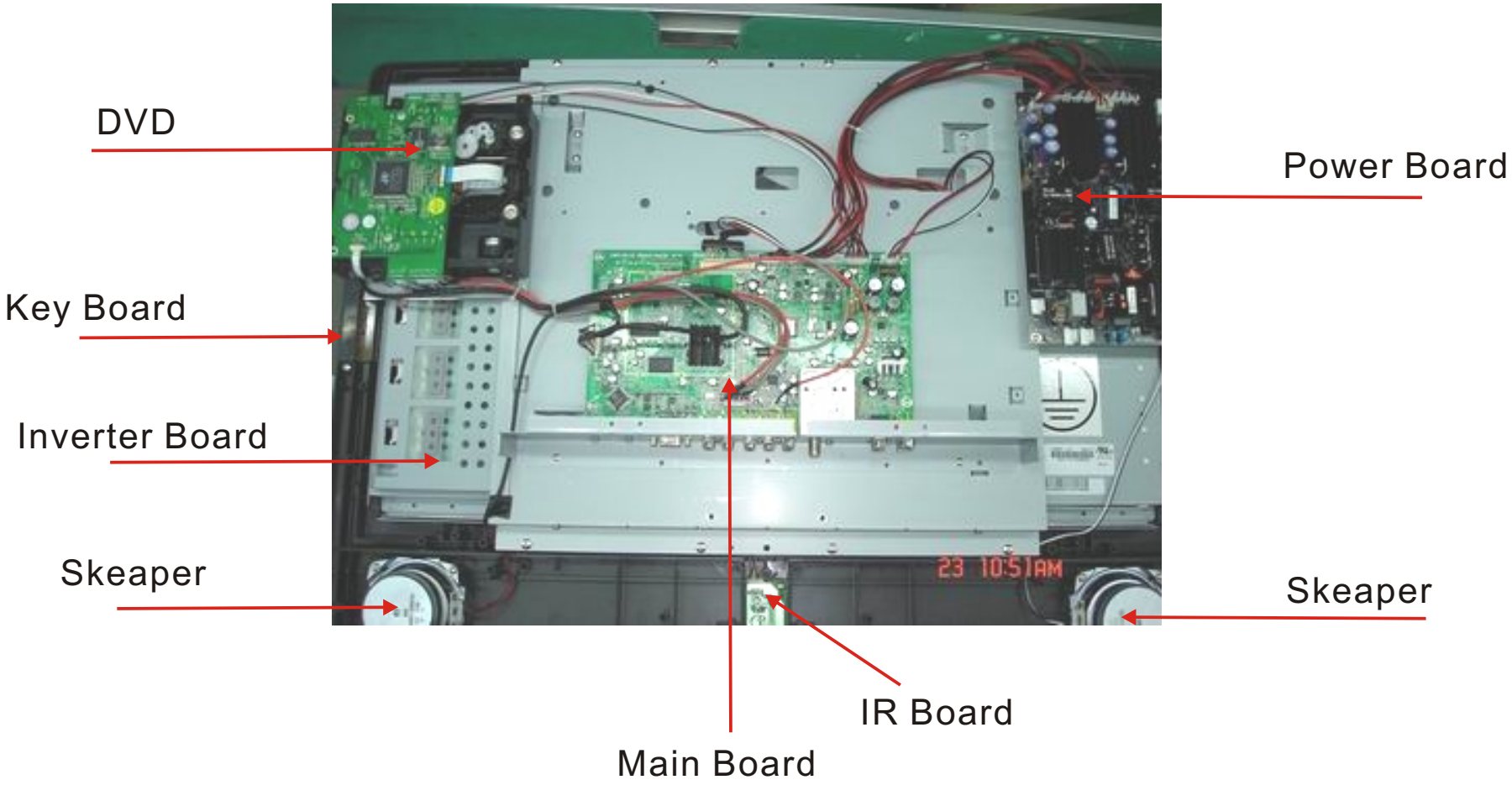
MT1389
MPEG decoder
&Servo System

SDRAM
64M

EEPROM

Flash
16M

Parts Position

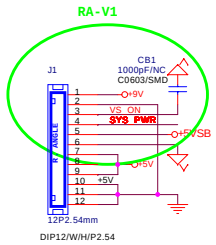


MT5372RAV6

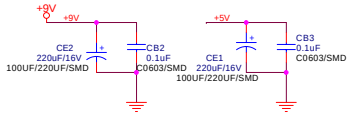
MT5372 (PBGA) REFERENCE DESIGN - 4 LAYERS

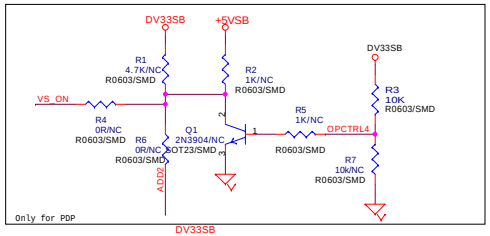
Rev	History	DATE
RA-V0	INITIAL VERSION	2006/07/14
RA-V1		2006/07/31
RA-V2		

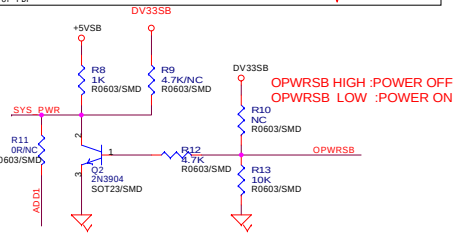
NAME	TYPE	DEVICE
+24V	POWER +24V	POWER SUPPLY
+12V	POWER +12V	POWER SUPPLY
+5V	POWER +5V	POWER SUPPLY
+5VSB	POWER +5V	POWER SUPPLY
DV33SB	POWER +3.3V	STANDBY POWER
+5V_TUENR	POWER +5V	TUNER POWER
DV33_DM	POWER +3.3V	MT5112 POWER AND ITS PERIPHERAL
DV18_DM	POWER +1.6V	MT5112 POWER
DV33	POWER +3.3V	MT5372 POWER AND ITS PERIPHERAL
AV33	POWER +3.3V	MT5372 ANALOG POWER
DV18_DDR	POWER +1.8V	MT5372 DDR POWER
AV15	POWER +1.5V	MT5372 VIDEO FRONT-END POWER
DV12	POWER +1.2V	MT5372 POWER
AV12	POWER +1.2V	MT5372 ANALOG POWER
GND	GROUND	DIGITAL GROUND
AGND_PLL	GROUND	ANALOG GROUND
AGND_AFE	GROUND	ANALOG GROUND
AGND_HDMI	GROUND	ANALOG GROUND
AGND_LVDS	GROUND	ANALOG GROUND

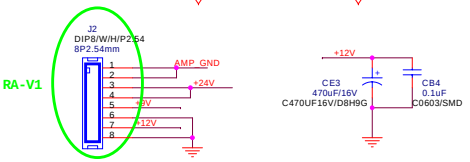


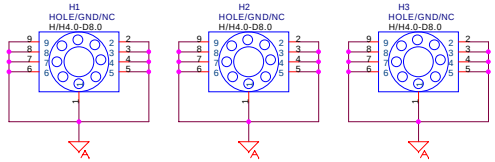
POWER INPUT

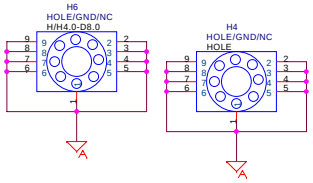


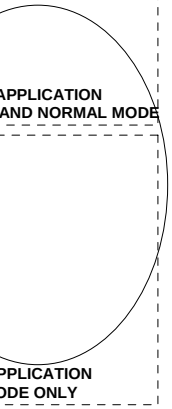




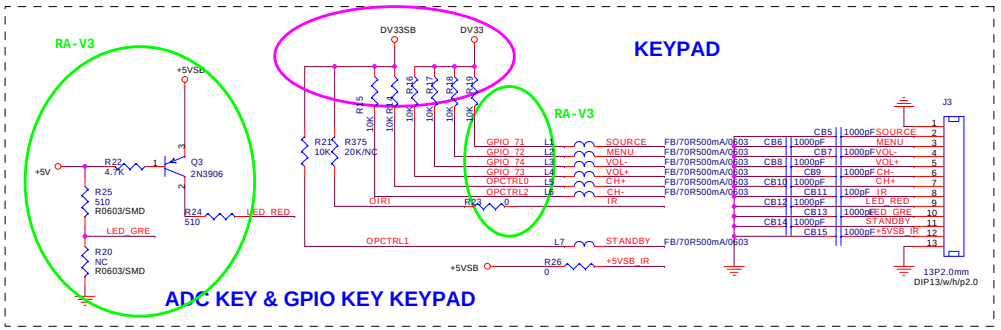


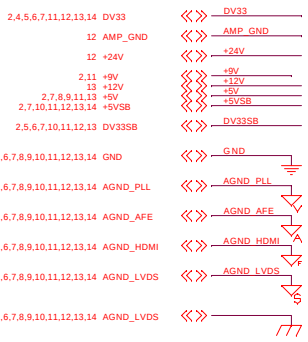






KEYPAD





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Title: INDEX

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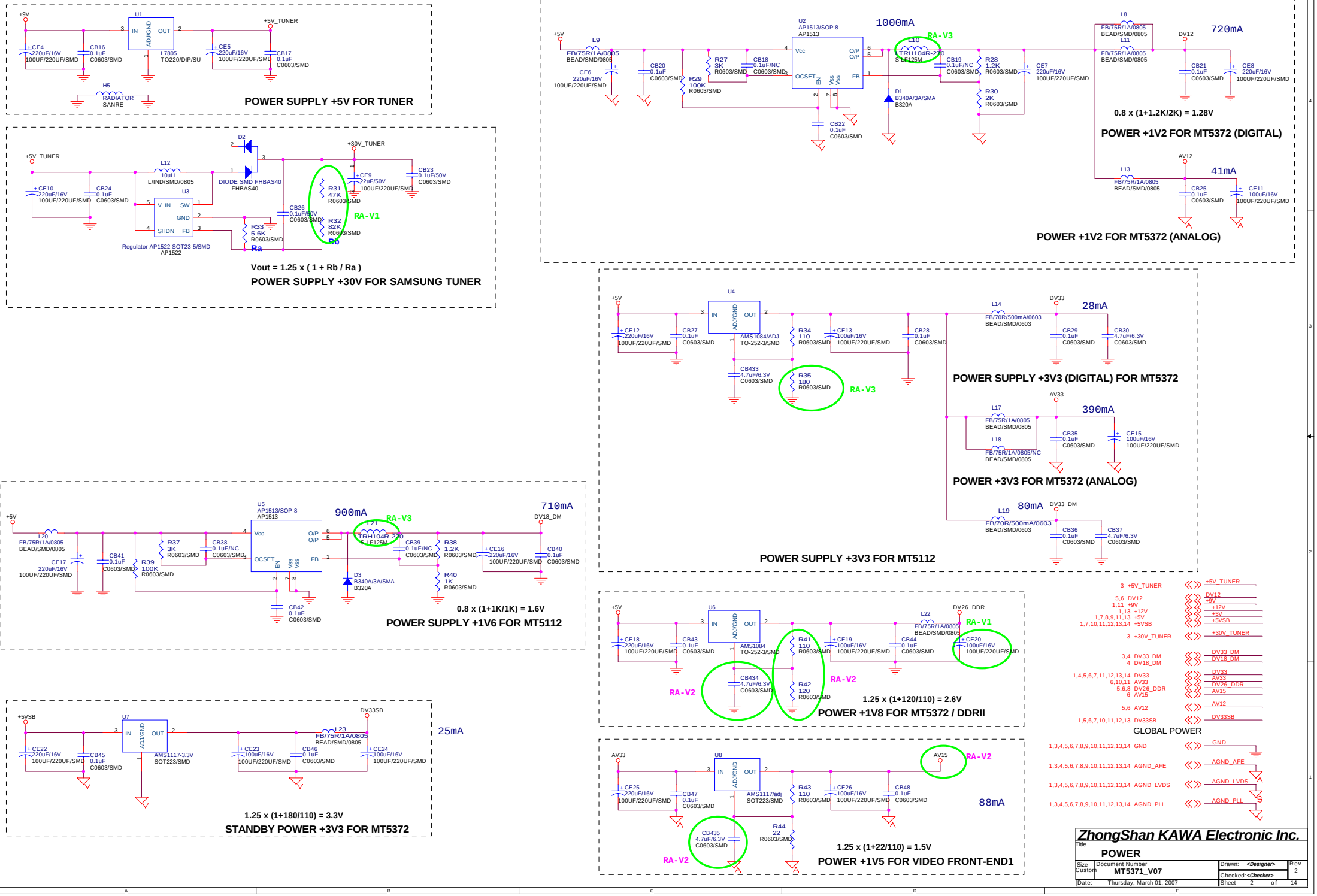
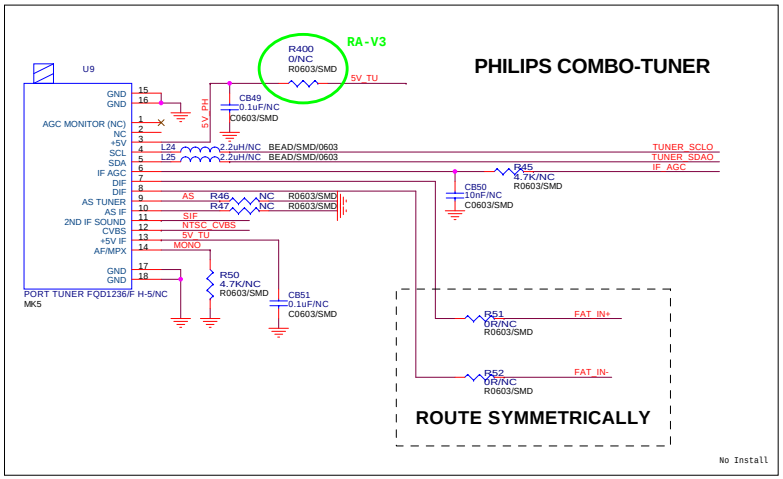
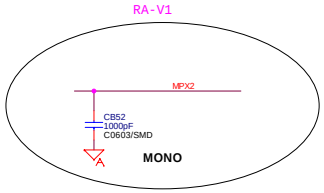
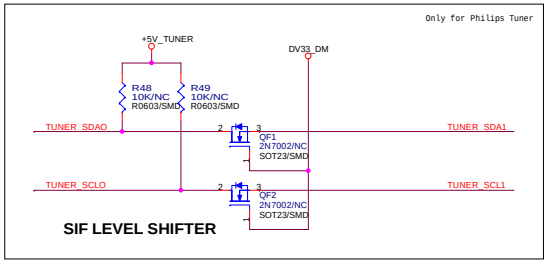
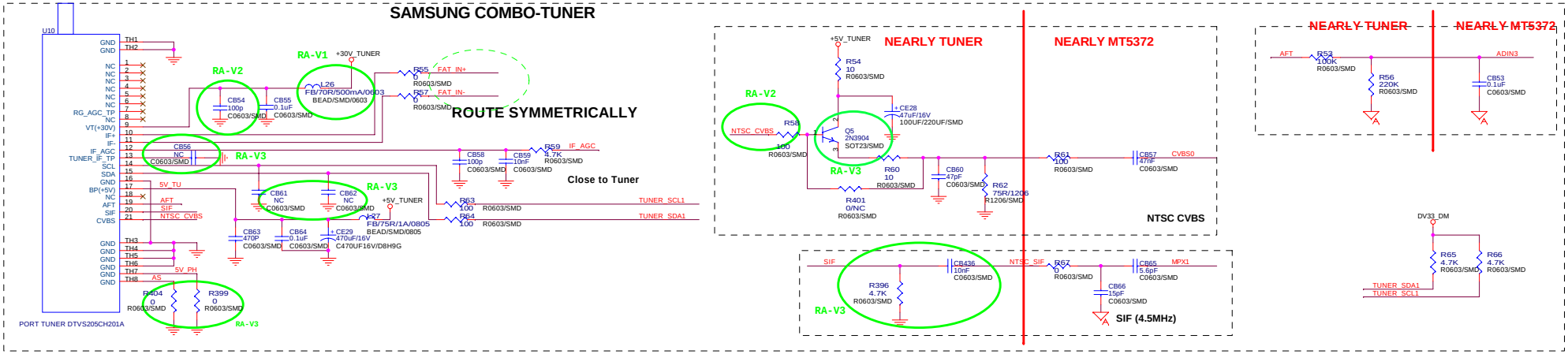
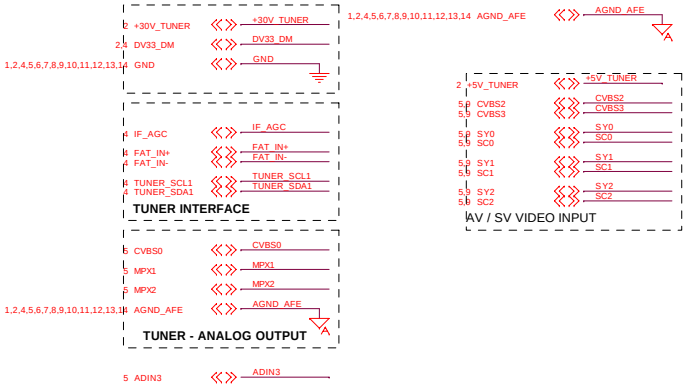

POWER SUPPLY +5V FOR TUNER
POWER SUPPLY +30V FOR SAMSUNG TUNER
Vout = 1.25 x (1 + Rb / Ra)
1000mA
720mA
0.8 x (1+1.2K/2K) = 1.28V
POWER +1V2 FOR MT5372 (DIGITAL)
41mA
POWER +1V2 FOR MT5372 (ANALOG)
28mA
POWER SUPPLY +3V3 (DIGITAL) FOR MT5372
390mA
POWER +3V3 FOR MT5372 (ANALOG)
80mA
POWER SUPPLY +3V3 FOR MT5112
900mA
710mA
0.8 x (1+1K/1K) = 1.6V
POWER SUPPLY +1V6 FOR MT5112
1.25 x (1+120/110) = 2.6V
POWER +1V8 FOR MT5372 / DDRII
88mA
1.25 x (1+22/110) = 1.5V
POWER +1V5 FOR VIDEO FRONT-END1
25mA
1.25 x (1+180/110) = 3.3V
STANDBY POWER +3V3 FOR MT5372
GLOBAL POWER
ZhongShan KAWA Electronic Inc.
POWER
MT5371_V07
Thursday, March 01, 2007











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Title: TUNER

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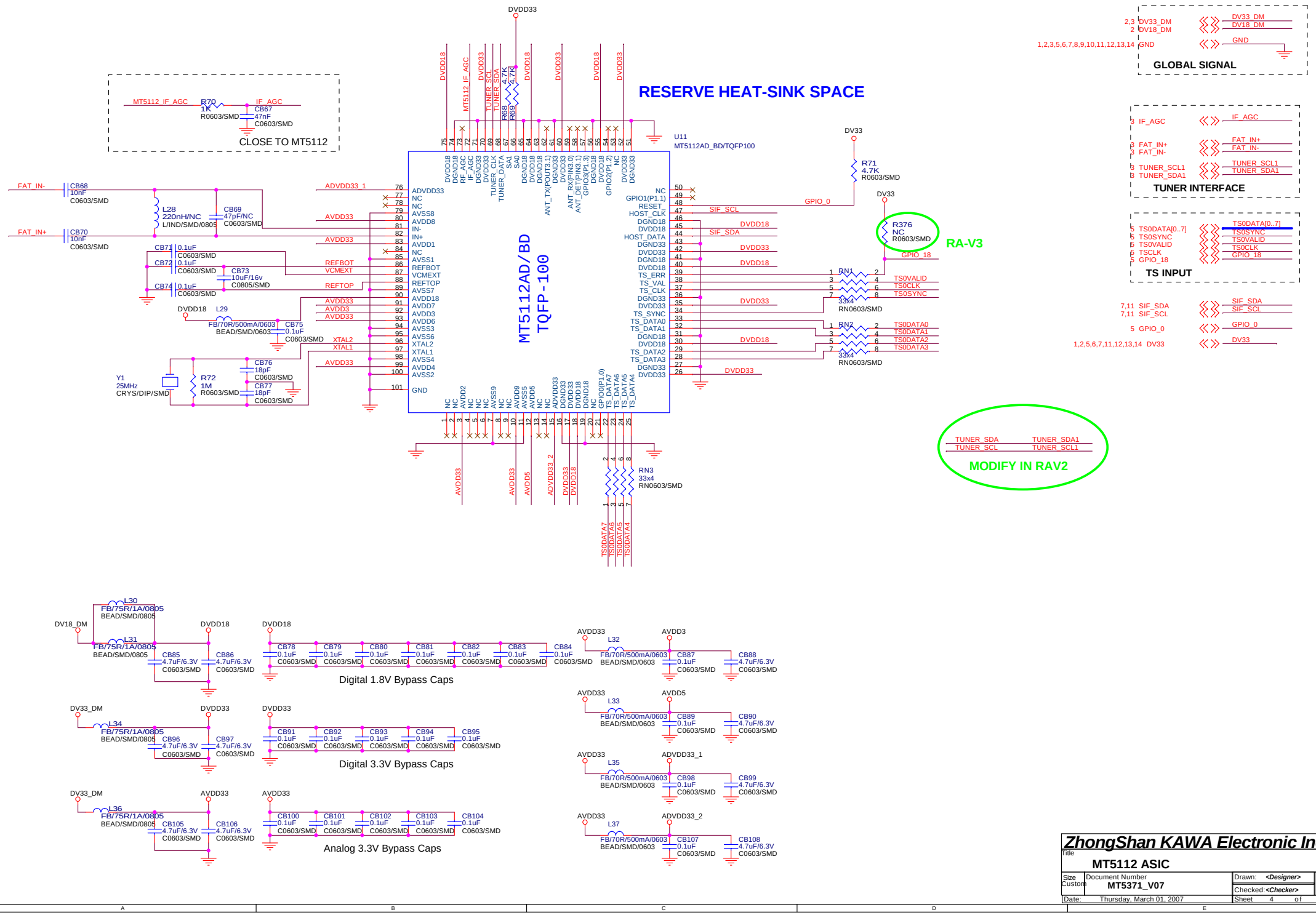
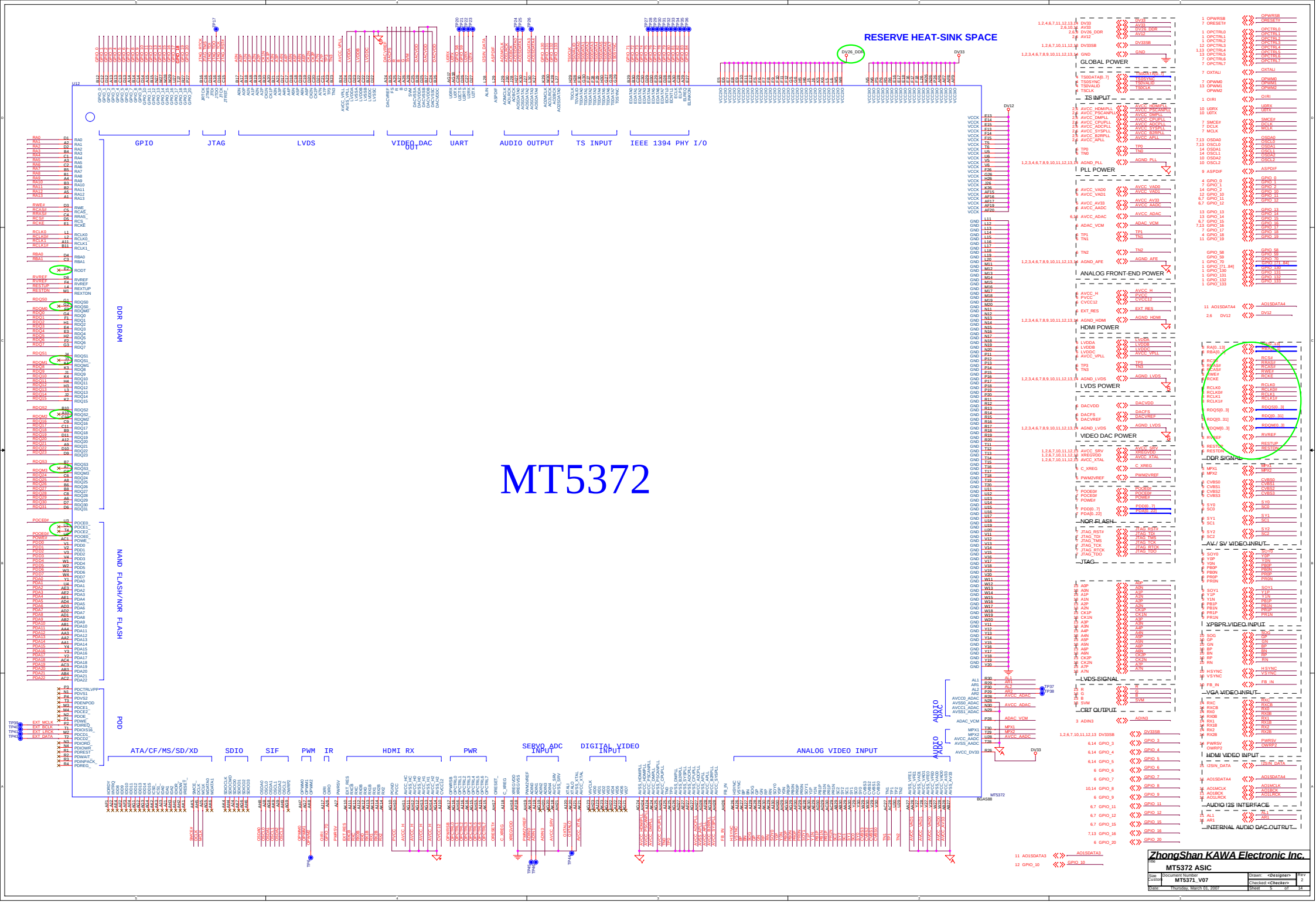
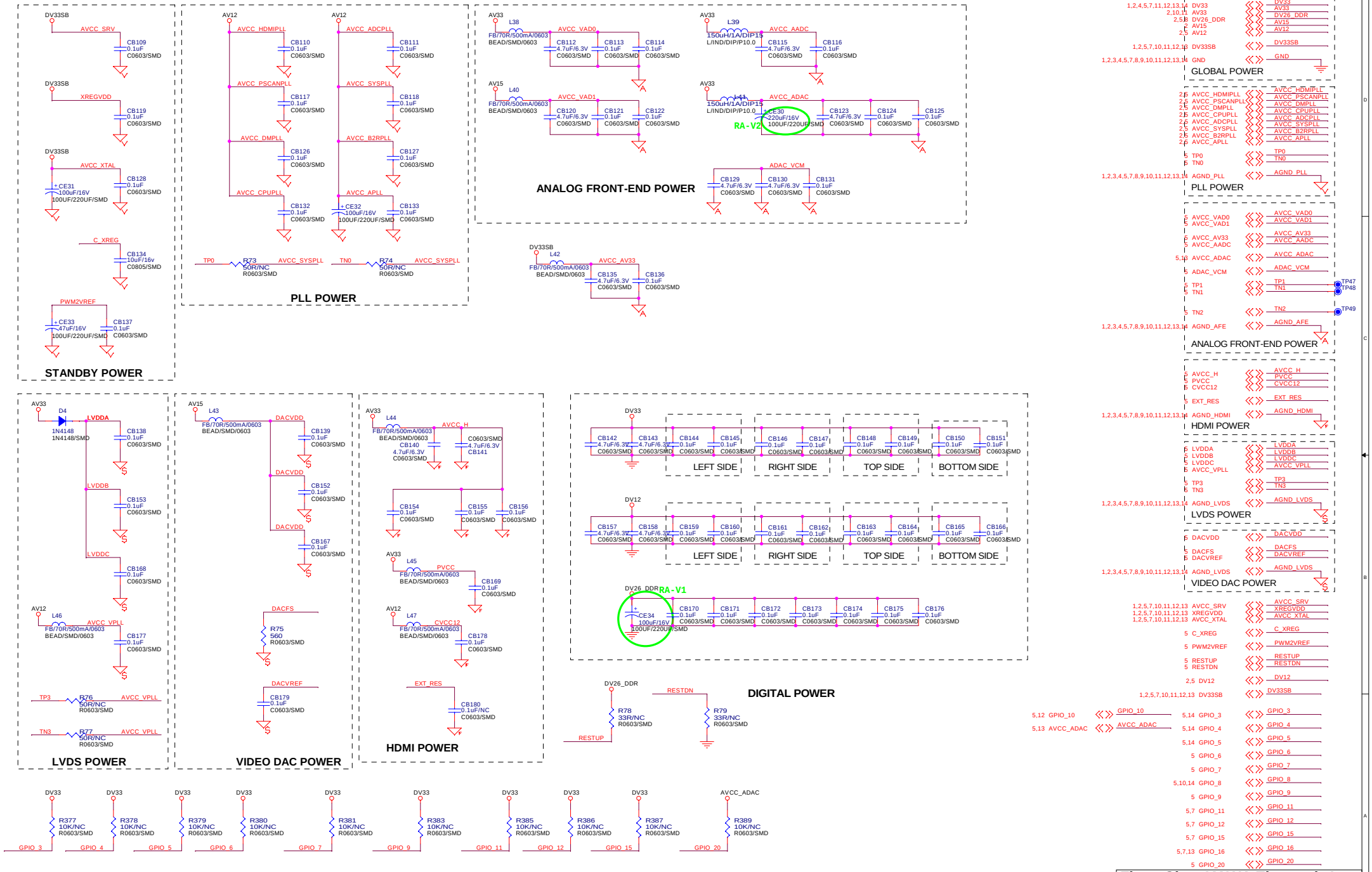
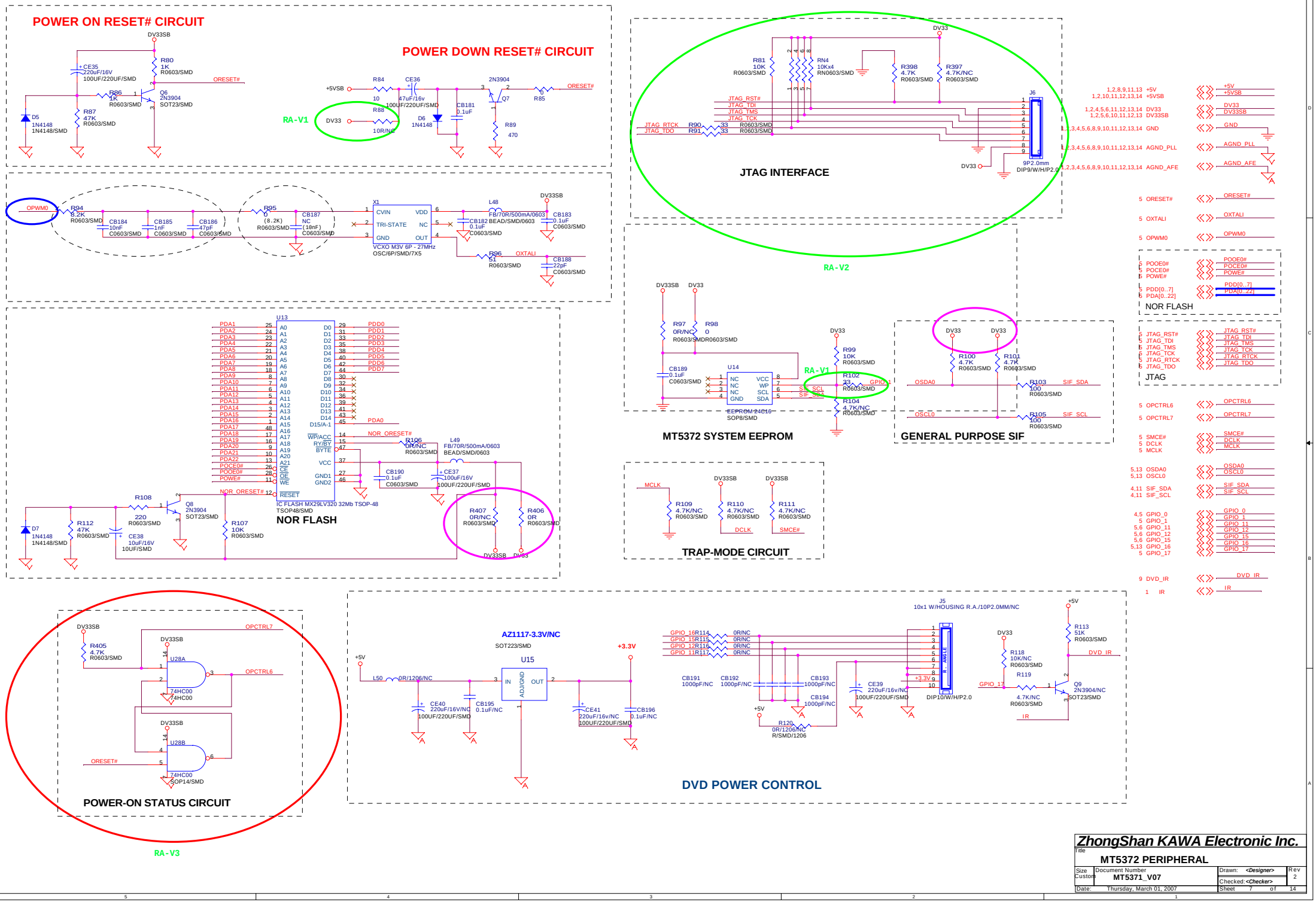
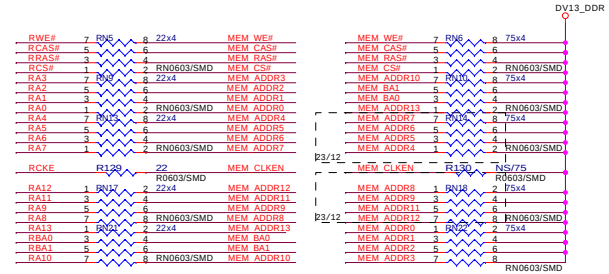

RESERVE HEAT-SINK SPACE
MT5112AD/BD
TQFP-100
U11
MT5112AD_BD/TQFP100
CLOSE TO MT5112
MT5112_IF_AGC
R70
1K
R0603/SMD
IF_AGC
CB67
47nF
C0603/SMD
DVDD33
DV33
R71
4.7K
R0603/SMD
R376
NC
R0603/SMD
RA-V3
GPIO_0
GPIO_18
SIF_SCL
SIF_SDA
FAT_IN-
FAT_IN+
CB68
10nF
C0603/SMD
CB70
10nF
C0603/SMD
L28
220nH/NC
L/IND/SMD/0805
CB69
47pF/NC
C0603/SMD
CB71
0.1uF
C0603/SMD
CB72
0.1uF
C0603/SMD
CB73
10uF/16v
C0805/SMD
CB74
0.1uF
C0603/SMD
REFBOT
VCMEXT
REFTOP
ADVDD33_1
AVDD33
AVDD3
DVDD18
L29
FB/70R/500mA/0603
BEAD/SMD/0603
CB75
0.1uF
C0603/SMD
XTAL2
XTAL1
Y1
25MHz
CRYS/DIP/SMD
R72
1M
R0603/SMD
CB76
18pF
C0603/SMD
CB77
18pF
C0603/SMD
RN1
RN2
RN3
33x4
RN0603/SMD
TS0VALID
TS0CLK
TS0SYNC
TS0DATA0
TS0DATA1
TS0DATA2
TS0DATA3
TS0DATA[0..7]
TUNER_SDA
TUNER_SCL
TUNER_SDA1
TUNER_SCL1
MODIFY IN RAV2
GLOBAL SIGNAL
DV33_DM
DV18_DM
GND
TUNER INTERFACE
IF_AGC
FAT_IN+
FAT_IN-
TUNER_SCL1
TUNER_SDA1
TS INPUT
SIF_SDA
SIF_SCL
DV33
L30
L31
L32
L33
L34
L35
L36
L37
FB/75R/1A/0805
BEAD/SMD/0805
FB/70R/500mA/0603
BEAD/SMD/0603
CB85
CB86
CB87
CB88
CB89
CB90
CB96
CB97
CB98
CB99
CB105
CB106
CB107
CB108
4.7uF/6.3V
C0603/SMD
Digital 1.8V Bypass Caps
Digital 3.3V Bypass Caps
Analog 3.3V Bypass Caps
ZhongShan KAWA Electronic Inc.
Title
MT5112 ASIC
Size
Custom
Document Number
MT5371_V07
Rev
1
Drawn: <Designer>
Checked: <Checker>
Date: Thursday, March 01, 2007
Sheet 4 of 14


MT5372
RESERVE HEAT-SINK SPACE
GPIO
JTAG
LVDS
VIDEO DAC OUT
UART
AUDIO OUTPUT
TS INPUT
IEEE 1394 PHY I/O
DDR DRAM
NAND FLASH/NOR FLASH
POD
ATA/CF/MS/SD/XD
SDIO
SIF
PWM
IR
HDMI RX
PWR
SERVO ADC INPUT
DIGITAL VIDEO INPUT
ANALOG VIDEO INPUT
AUDIO DAC
GLOBAL POWER
TS INPUT
PLL POWER
ANALOG FRONT-END POWER
HDMI POWER
LVDS POWER
VIDEO DAC POWER
NOR FLASH
JTAG
LVDS SIGNAL
CRT OUTPUT
DDR SIGNAL
AV / SV VIDEO INPUT
YPBPR VIDEO INPUT
VGA VIDEO INPUT
HDMI VIDEO INPUT
AUDIO I2S INTERFACE
INTERNAL AUDIO DAC OUTPUT
EXT_MCLK
EXT_BCLK
EXT_LRCK
EXT_DATA

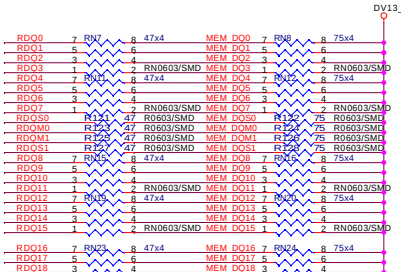

STANDBY POWER
PLL POWER
ANALOG FRONT-END POWER
LVDS POWER
VIDEO DAC POWER
HDMI POWER
DIGITAL POWER
GLOBAL POWER
PLL POWER
ANALOG FRONT-END POWER
HDMI POWER
LVDS POWER
VIDEO DAC POWER
RA-V2
RA-V1
LEFT SIDE
RIGHT SIDE
TOP SIDE
BOTTOM SIDE
ZhongShan KAWA Electronic Inc.
MT5372 BYPASS CAP.
MT5371_V07
Thursday, March 01, 2007


POWER ON RESET# CIRCUIT
POWER DOWN RESET# CIRCUIT
RA-V1
JTAG INTERFACE
RA-V2
MT5372 SYSTEM EEPROM
GENERAL PURPOSE SIF
NOR FLASH
TRAP-MODE CIRCUIT
POWER-ON STATUS CIRCUIT
RA-V3
DVD POWER CONTROL
AZ1117-3.3V/NC
ZhongShan KAWA Electronic Inc.
MT5372 PERIPHERAL
MT5371_V07
Thursday, March 01, 2007



CLOSED TO MT5372 CLOSED TO DDR

CLOSED TO MT5372 CLOSED TO DDR



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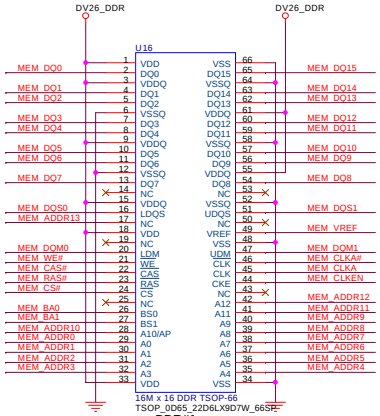
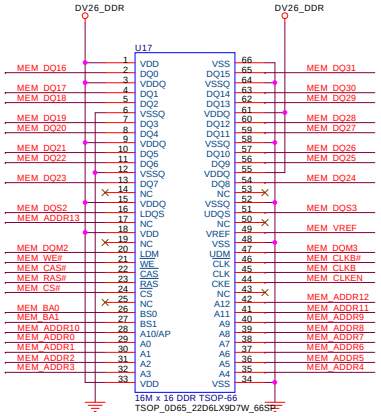
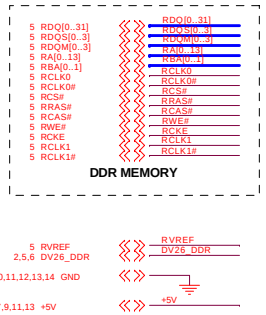
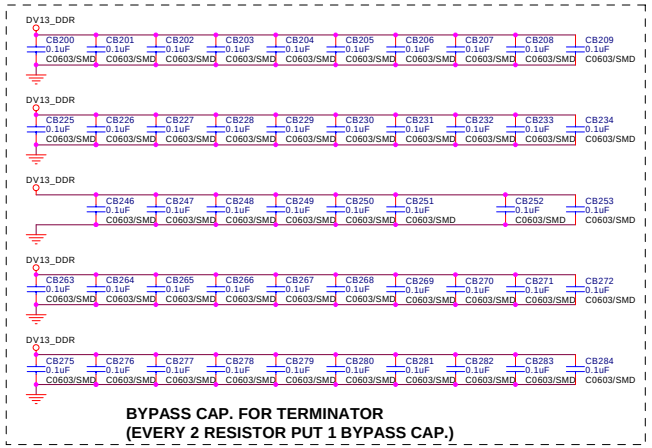


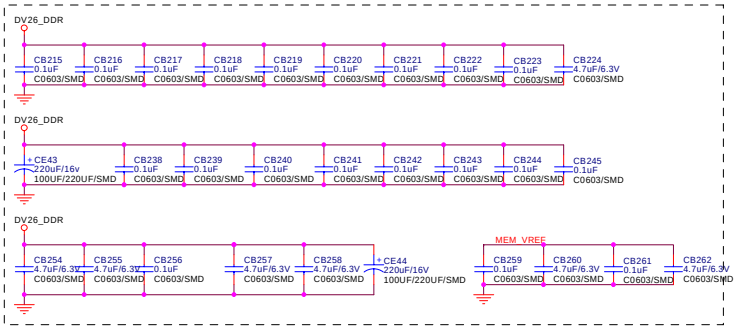
DDR#1

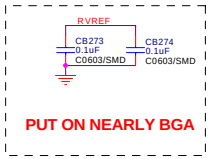




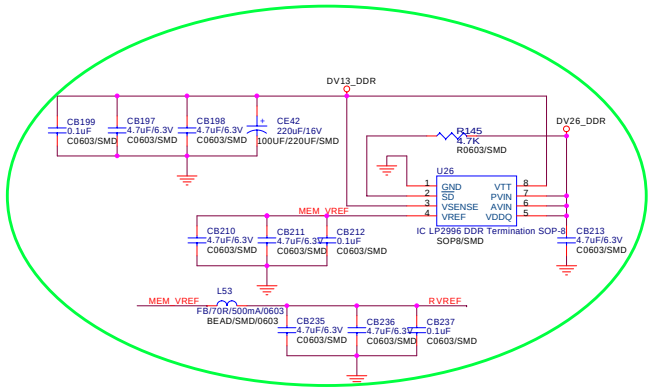


BYPASS CAP. FOR TERMINATOR
(EVERY 2 RESISTOR PUT 1 BYPASS CAP.)



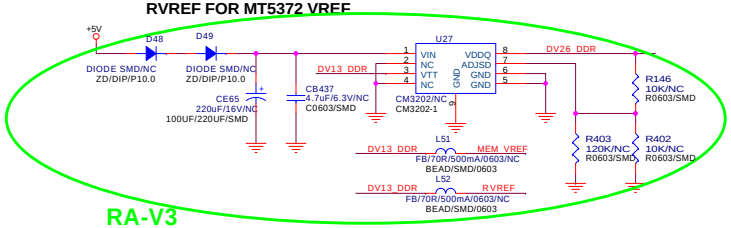


PUT ON NEARLY BGA



RA-V3

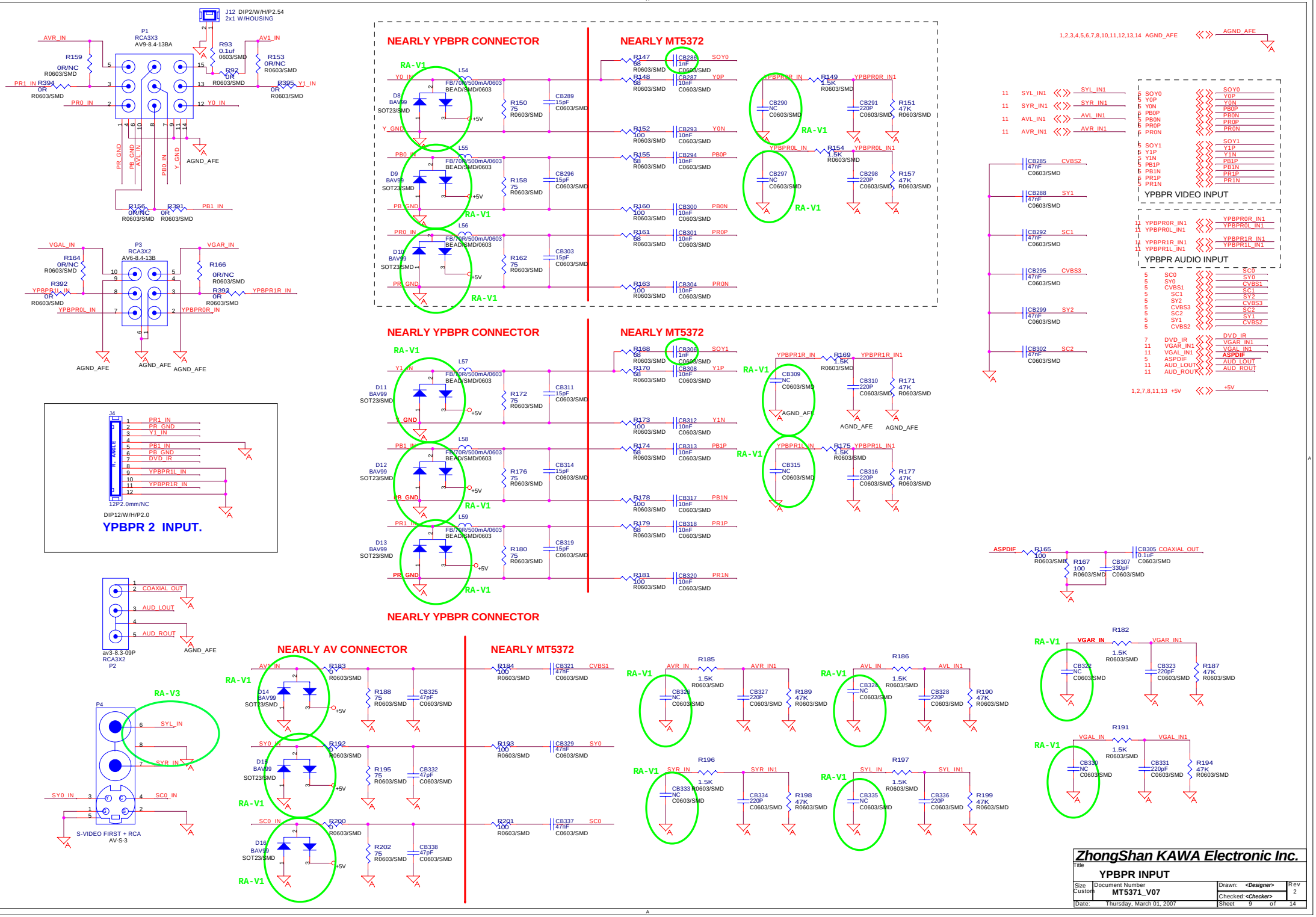
BYPASS CAP. FOR DIMM
DV13_DDR FOR DDR TERMINATOR
MEM_VREF FOR DDR VREF
RVREF FOR MT5372 VREF



RA-V3

ZhongShan KAWA Electronic Inc.

Title: DDR1 MEMORY			
Size: Custom	Document Number: MT5371_V07	Drawn: <Designer>	Rev: 1
		Checked: <Checker>	
Date: Thursday, March 01, 2007		Sheet 8 of 14	


NEARLY YPBPR CONNECTOR
NEARLY MT5372
NEARLY YPBPR CONNECTOR
NEARLY MT5372
NEARLY YPBPR CONNECTOR
NEARLY AV CONNECTOR
NEARLY MT5372
YPBPR 2 INPUT.
YPBPR VIDEO INPUT
YPBPR AUDIO INPUT
S-VIDEO FIRST + RCA
AV-S-3
ZhongShan KAWA Electronic Inc.
YPBPR INPUT
MT5371_V07
Thursday, March 01, 2007

DEL; CB339_R203_R206_R207_U19

AV33 AV33

R204 10K R0603/SMD

R205 10K R0603/SMD

OSCL2 OSDA2

PULL HIGH AV33

HDMI HDCP EEPROM

2006.12.16

DEL: D17~D27_D60_P5_U20_Q10_Q19_CB340

DEL: R36_RR82_R83_R208_R209_R210_R211_R212_R216_R217_R218_R390_R408

2006.12.16

1,2,4,5,6,7,11,12,13,14 DV33 — DV33

1,2,7,8,9,11,13 +5V — +5V

1,2,5,6,7,11,12,13 DV33SB — DV33SB

2,6,11 AV33 — AV33

2,6 AV15 — AV15

1,2,3,4,5,6,7,8,9,11,12,13,14 AGND_HDMI — AGND_HDMI

1,2,3,4,5,6,7,8,9,11,12,13,14 AGND_AFE — AGND_AFE

5 OSDA2 — OSDA2

5 OSCL2 — OSCL2

SIF INTERFACE

OWRP2 — OWRP2

5,14 GPIO_8 — GPIO_8

5,14 GPIO_2 — GPIO_2

5,7,13 GPIO_16 — GPIO_16

DEL: R214_R219_R215_R213_U21_R225_R226

2006.12.16

VGASCL_IN — R222 100 R0603/SMD — VGASCL

R220 20K R0603/SMD

D28 BAV99 SOT23/SMD — RA-V1

CB342 NC/47PF C0603/SMD

VGA_PLUGPWR

VGASDA_IN — R223 100 R0603/SMD — VGASDA

R221 20K R0603/SMD

D29 BAV99 SOT23/SMD — RA-V1

CB343 NC/47PF C0603/SMD

VGA_PLUGPWR

VGA_PLUGPWR

CB341 0.1uF C0603/SMD

U22

NC NC NC GND — VCC WP SCL SDA

EEPROM 24C04 SOP8/SMD

VGAROMWP VGASCL VGASDA

R224 20K R0603/SMD

R228 10K/NC R0603/SMD

R227 33 R0603/SMD — GPIO_8

H : WP ENABLE
L : WP DISABLE

RA-V3

NEARLY VGA CONNECTOR | **NEARLY MT5372**

GRN — L60 FB/70R/500mA/0603 BEAD/SMD/0603 — D30 BAV99 SOT23/SMD — RA-V1 — GRN_GND

R231 75 R0603/SMD — CB346 5pF C0603/SMD — VGA_PLUGPWR

R229 68 R0603/SMD — CB344 1nF C0603/SMD — SOG

R230 68 R0603/SMD — CB345 10nF C0603/SMD — GP

BLU — L62 FB/70R/500mA/0603 BEAD/SMD/0603 — D32 BAV99 SOT23/SMD — RA-V1 — BLU_GND

R236 75 R0603/SMD — CB350 5pF C0603/SMD — VGA_PLUGPWR

R232 100 R0603/SMD — CB347 10nF C0603/SMD — GN

R234 68 R0603/SMD — CB348 10nF C0603/SMD — BP

RED — L63 FB/70R/500mA/0603 BEAD/SMD/0603 — D33 BAV99 SOT23/SMD — RA-V1 — RED_GND

R240 75 R0603/SMD — CB353 5pF C0603/SMD — VGA_PLUGPWR

R237 100 R0603/SMD — CB351 10nF C0603/SMD — BN

R238 68 R0603/SMD — CB352 10nF C0603/SMD — RP

R242 100 R0603/SMD — CB355 10nF C0603/SMD — RN

1,2,7,11,12,13,14 +5VSB — +5VSB

1,2,5,6,7,11,12,13 DV33SB — DV33SB

2,6,11 AV33 — AV33

1,2,3,4,5,6,7,8,9,11,12,13,14 AGND_AFE — AGND_AFE

5 SOG — SOG

5 GP — GP

5 GN — GN

5 BP — BP

5 BN — BN

5 RP — RP

5 RN — RN

5 HSYNC — HSYNC

5 VSYNC — VSYNC

5 FB_IN — FB_IN — TP50

VGA VIDEO INPUT

HSYNC# — R233 510 R0603/SMD — L61 2.2uH BEAD/SMD/0603 — HSYNC

D31 BAV99 SOT23/SMD — RA-V1

R235 2K R0603/SMD — CB349 5pF C0603/SMD — VGA_PLUGPWR

VSYNC# — R239 510 R0603/SMD — L64 2.2uH BEAD/SMD/0603 — VSYNC

D34 BAV99 SOT23/SMD — RA-V1

R241 2K R0603/SMD — CB354 5pF C0603/SMD — VGA_PLUGPWR

5 U0TX — U0TX

5 U0RX — U0RX

5,7 GPIO_1 — GPIO_1

1,2,3,4,5,6,7,8,9,11,12,13,14 AGND_PLL — AGND_PLL

RXD 11 — RED_GND 6 — RED 1 — GRN_GND 7 — GRN 2 — BLU_GND 8 — BLU 3 — TXD 9 — 4 — 10 — 5

VGASDA_IN 12

HSYNC# 13

VSYNC# 14

VGASCL_IN 15

16 — 17

P6 D-SUB15 FEMALE DSUB15/DIP/F

D36 1N4148 1N4148/SMD — VGA_PLUGPWR

+5VSB — D35 1N4148 1N4148/SMD

CB356 1uF/16v C0603/SMD — CB357 1uF/16v C0603/SMD — CB358 1uF/16v C0603/SMD — RA-V1

DV33SB

R245 0 R0603/SMD — U0RX

RXD — D37 BAV99 SOT23/SMD — RA-V1 — +5VSB

R243 4.7K R0603/SMD — R244 4.7K R0603/SMD

J8 — 4P2.0mm — DIP4/W/H/P2.0

TXD — U0TX — R246 0 R0603/SMD

CB359 22pF C0603/SMD — CB360 22pF C0603/SMD

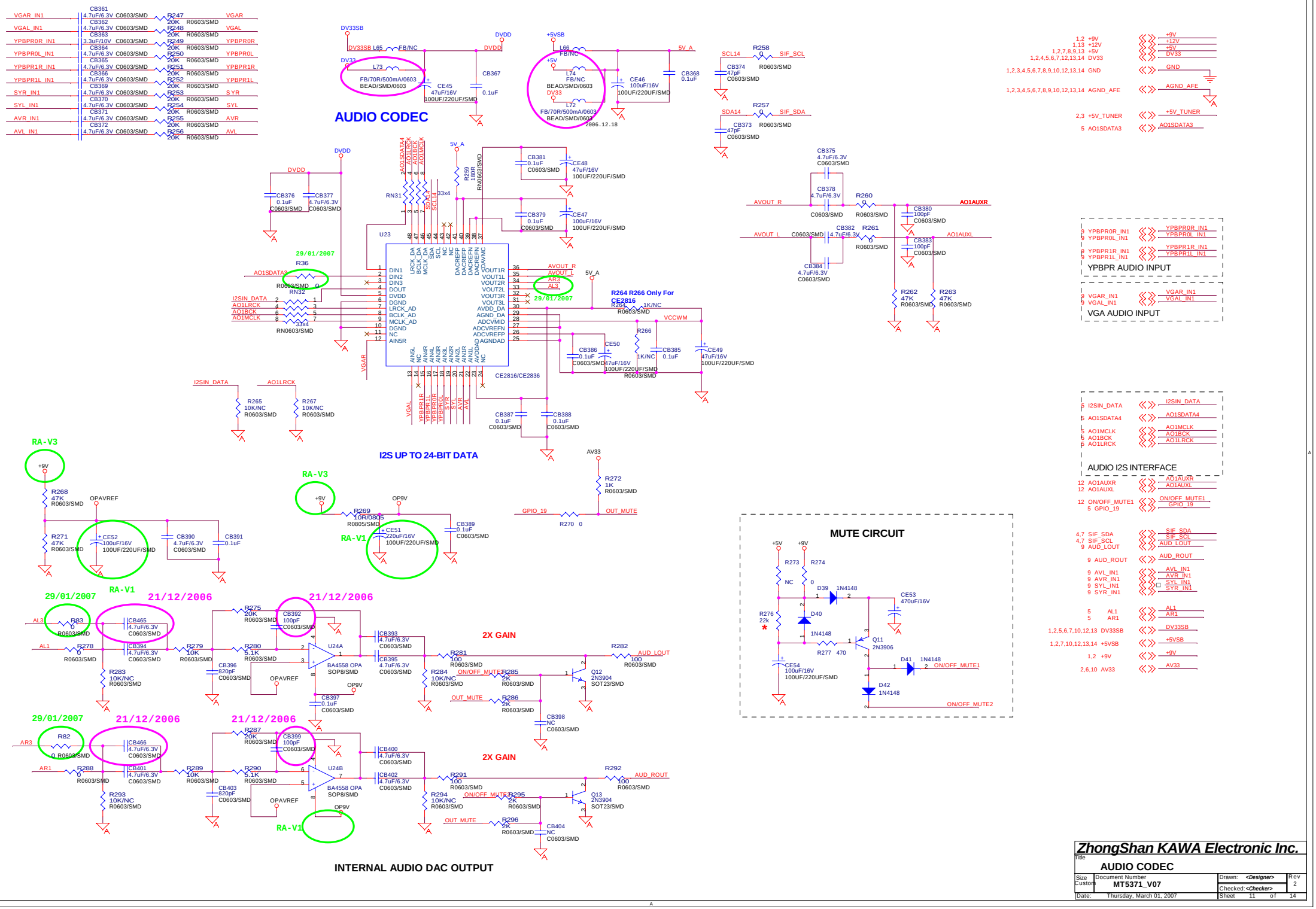
D38 BAV99 SOT23/SMD — +5VSB — RA-V1

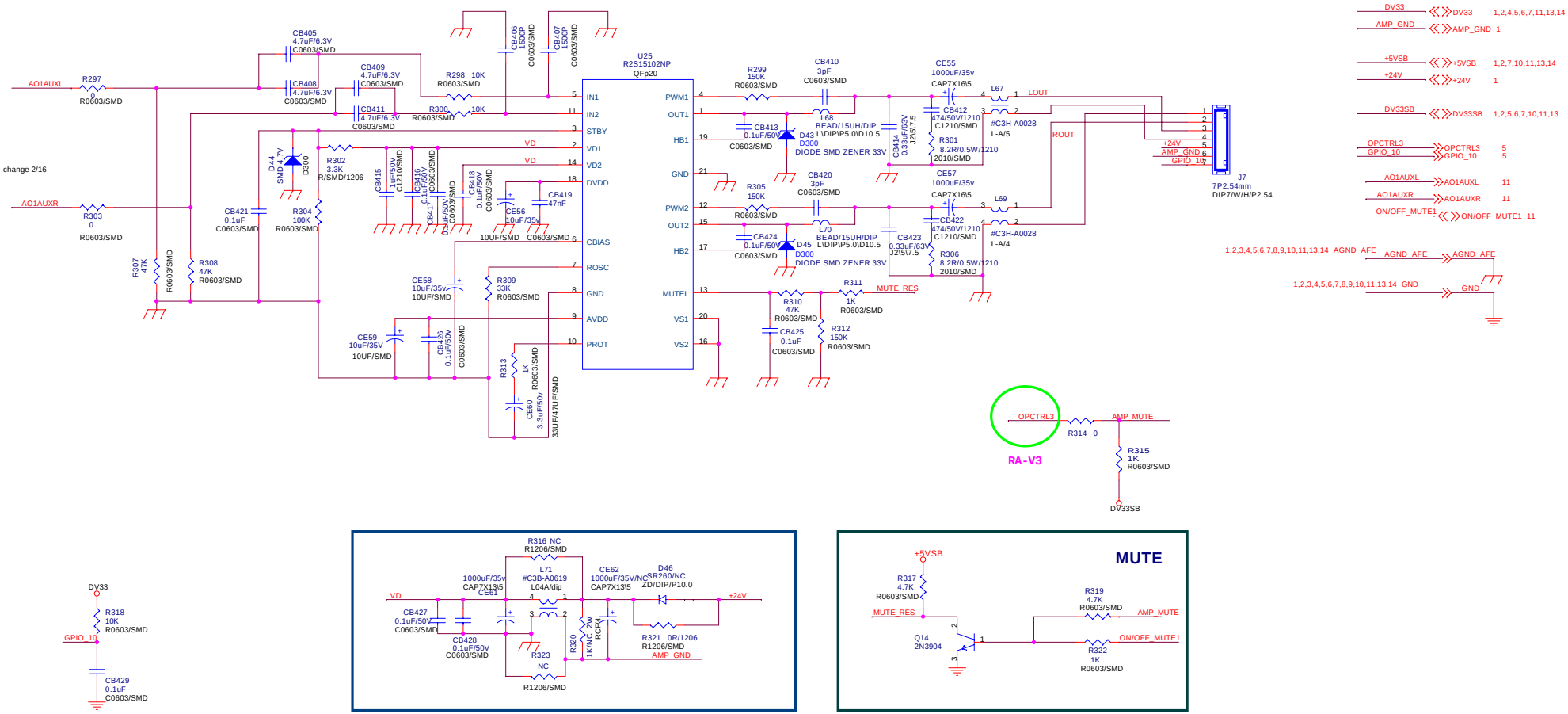
FOR CODE DOWNLOAD AND DEBUGGING

ZhongShan KAWA Electronic Inc.

Title: **HDMI /VGA INPUT**

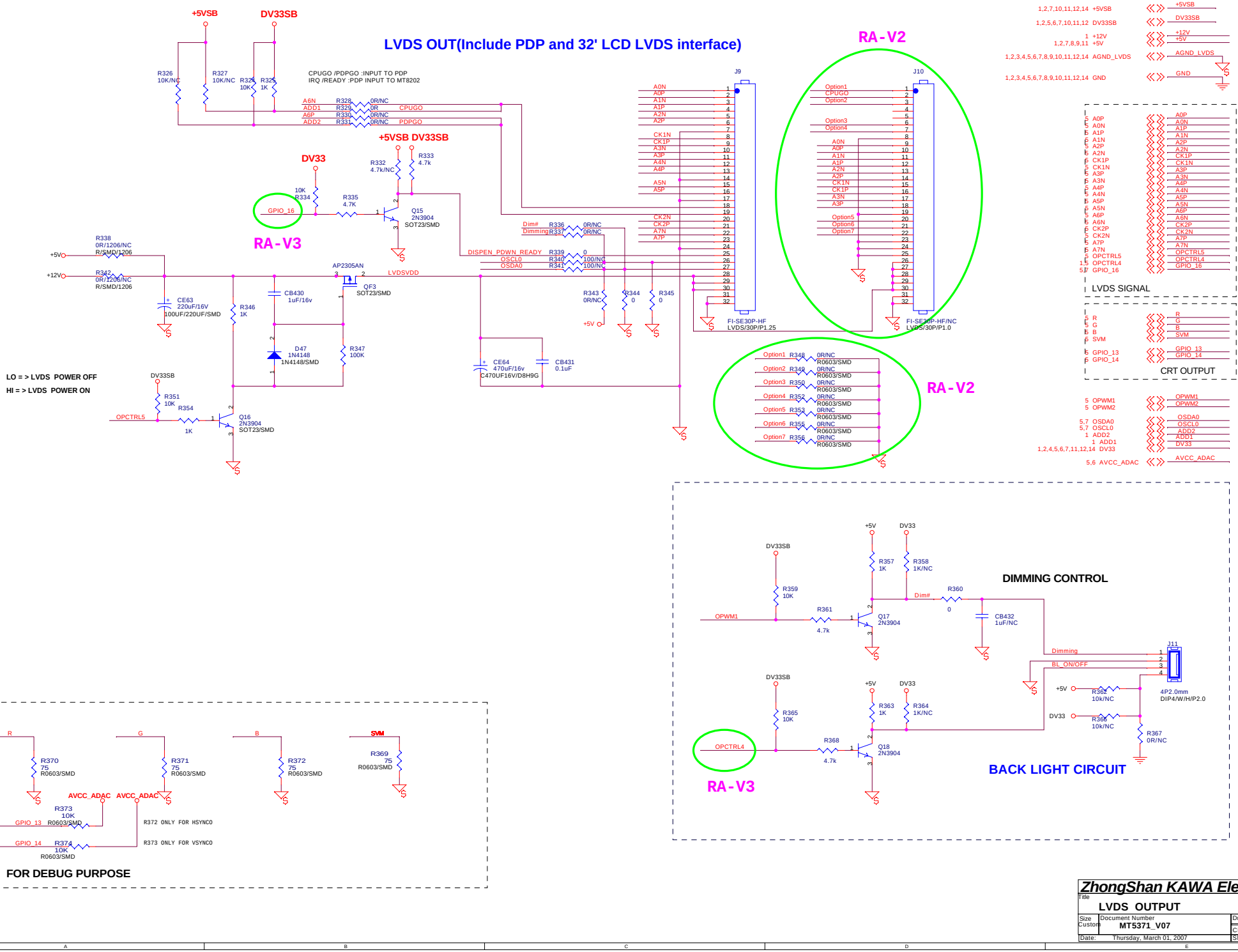
Size	Document Number	Drawn	Rev
Custom	MT5371_V07	<Designer>	1
		Checked: <Checker>	
Date: Thursday, March 01, 2007		Sheet 10 of 14	

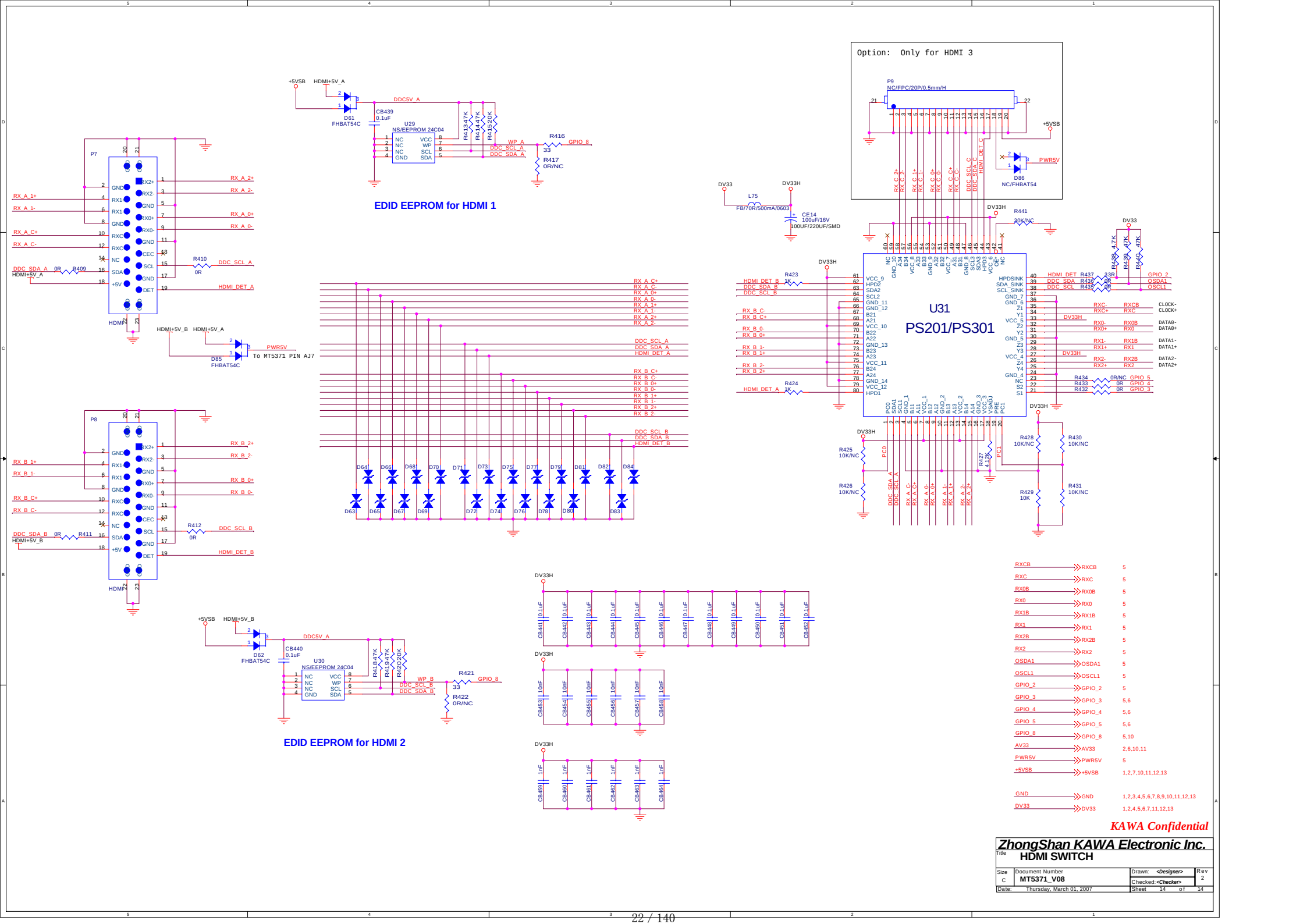

AUDIO CODEC
I2S UP TO 24-BIT DATA
INTERNAL AUDIO DAC OUTPUT
MUTE CIRCUIT
YPBPR AUDIO INPUT
VGA AUDIO INPUT
AUDIO I2S INTERFACE
R264 R266 Only For CE2816
2X GAIN
RA-V3
RA-V1
29/01/2007
21/12/2006
ZhongShan KAWA Electronic Inc.
AUDIO CODEC
MT5371_V07
Thursday, March 01, 2007



GPIO8: SPEAKER SWITCH(INTERNAL OR EXTERNAL

ZhongShan KAWA Electronic Inc.			
Title: AUDIO AMP			
Size: Custom	Document Number: MT5371_V07	Drawn: <Designer>	Rev: 1
		Checked: <Checker>	
Date: Thursday, March 01, 2007		Sheet 12 of 14	


LVDS OUT(Include PDP and 32' LCD LVDS interface)
RA-V2
RA-V3
RA-V2
+5VSB
DV33SB
CPUGO /PDPGO :INPUT TO PDP
IRQ /READY :PDP INPUT TO MT8202
R326 10K/NC
R327 10K/NC
R324 10K
R325 1K
A6N R328 0R/NC
ADD1 R329 0R CPUGO
A6P R330 0R/NC
ADD2 R331 0R/NC PDPGO
+5VSB DV33SB
DV33
R332 4.7k/NC
R333 4.7k
10K R334
R335 4.7K
GPIO_16
Q15 2N3904 SOT23/SMD
Dim# R336 0R/NC
Dimming R337 0R/NC
DISPEN_PDWN_READY R339 0
OSCL0 R340 100/NC
OSDA0 R341 100/NC
R338 0R/1206/NC R/SMD/1206
R342 0R/1206/NC R/SMD/1206
+5V
+12V
AP2305AN
QF3 SOT23/SMD
LVDSVDD
CE63 220uF/16V 100UF/220UF/SMD
R346 1K
CB430 1uF/16v
D47 1N4148 1N4148/SMD
R347 100K
CE64 470uF/16v C470UF16V/D8H9G
CB431 0.1uF
R343 0R/NC
R344 0
R345 0
LO = > LVDS POWER OFF
HI = > LVDS POWER ON
DV33SB
R351 10K
R354 1K
OPCTRL5
Q16 2N3904 SOT23/SMD
J9
FI-SE30P-HF LVDS/30P/P1.25
J10
FI-SE30P-HF/NC LVDS/30P/P1.0
Option1 R348 0R/NC R0603/SMD
Option2 R349 0R/NC R0603/SMD
Option3 R350 0R/NC R0603/SMD
Option4 R352 0R/NC R0603/SMD
Option5 R353 0R/NC R0603/SMD
Option6 R355 0R/NC R0603/SMD
Option7 R356 0R/NC R0603/SMD
1,2,7,10,11,12,14 +5VSB
1,2,5,6,7,10,11,12 DV33SB
1 +12V
1,2,7,8,9,11 +5V
1,2,3,4,5,6,7,8,9,10,11,12,14 AGND_LVDS
1,2,3,4,5,6,7,8,9,10,11,12,14 GND
LVDS SIGNAL
CRT OUTPUT
5 OPWM1
5 OPWM2
5,7 OSDA0
5,7 OSCL0
1 ADD2
1 ADD1
1,2,4,5,6,7,11,12,14 DV33
5,6 AVCC_ADAC
DIMMING CONTROL
R357 1K
R358 1K/NC
R359 10K
R360 0
R361 4.7k
Q17 2N3904
CB432 1uF/NC
Dimming
BL_ON/OFF
J11
4P2.0mm DIP4/W/H/P2.0
R362 10k/NC
R366 10k/NC
R367 0R/NC
R363 1K
R364 1K/NC
R365 10K
R368 4.7k
Q18 2N3904
BACK LIGHT CIRCUIT
R
G
B
SVM
R370 75 R0603/SMD
R371 75 R0603/SMD
R372 75 R0603/SMD
R369 75 R0603/SMD
AVCC_ADAC
R373 10K
R374 10K R0603/SMD
R372 ONLY FOR HSYNCO
R373 ONLY FOR VSYNCO
FOR DEBUG PURPOSE
ZhongShan KAWA Electronic Inc.
LVDS OUTPUT
Size Custom
Document Number MT5371_V07
Drawn: <Designer>
Checked: <Checker>
Rev 2
Date: Thursday, March 01, 2007
Sheet 13 of 14



KAWA Confidential

Company	ZhongShan KAWA Electronic Inc.
Title	HDMI SWITCH
Size	C
Document Number	MT5371_V08
Drawn	<Designer>
Checked	<Checker>
Rev	2
Date	Thursday, March 01, 2007
Sheet	14 of 14

Basic operation of TFT-LCD

1. After turning on power switch, PSU board sends 5Vst-by Volt to Main IC MT5371 waiting for ON signals from Key Switch or Remote Receiver.

2. When the ON signal from Key Switch or Remote Receiver is detected, MT5371 will send ON Control signals to Power. Then Sub PSU sends 5Vsc, 9Vsc, 24V to PCBs working.

3. If some abnormal signals are detected (for example: over volts, over current, over temperature and under volts), the system will be shut down by Power off.

Main IC Specifications

- MT537x Application Note

- MT5112BD

- CE2836
  24-bit, 192KHz. CODEC: 6 ch DAC, 5 Input Mux Stereo ADC

- R2S15102NP
  Digital Power Amplifier R2S15102NP

Specifications are subject to change without notice

MT537x Application Note

V 0.5

Specifications are subject to change without notice

1. Revision History

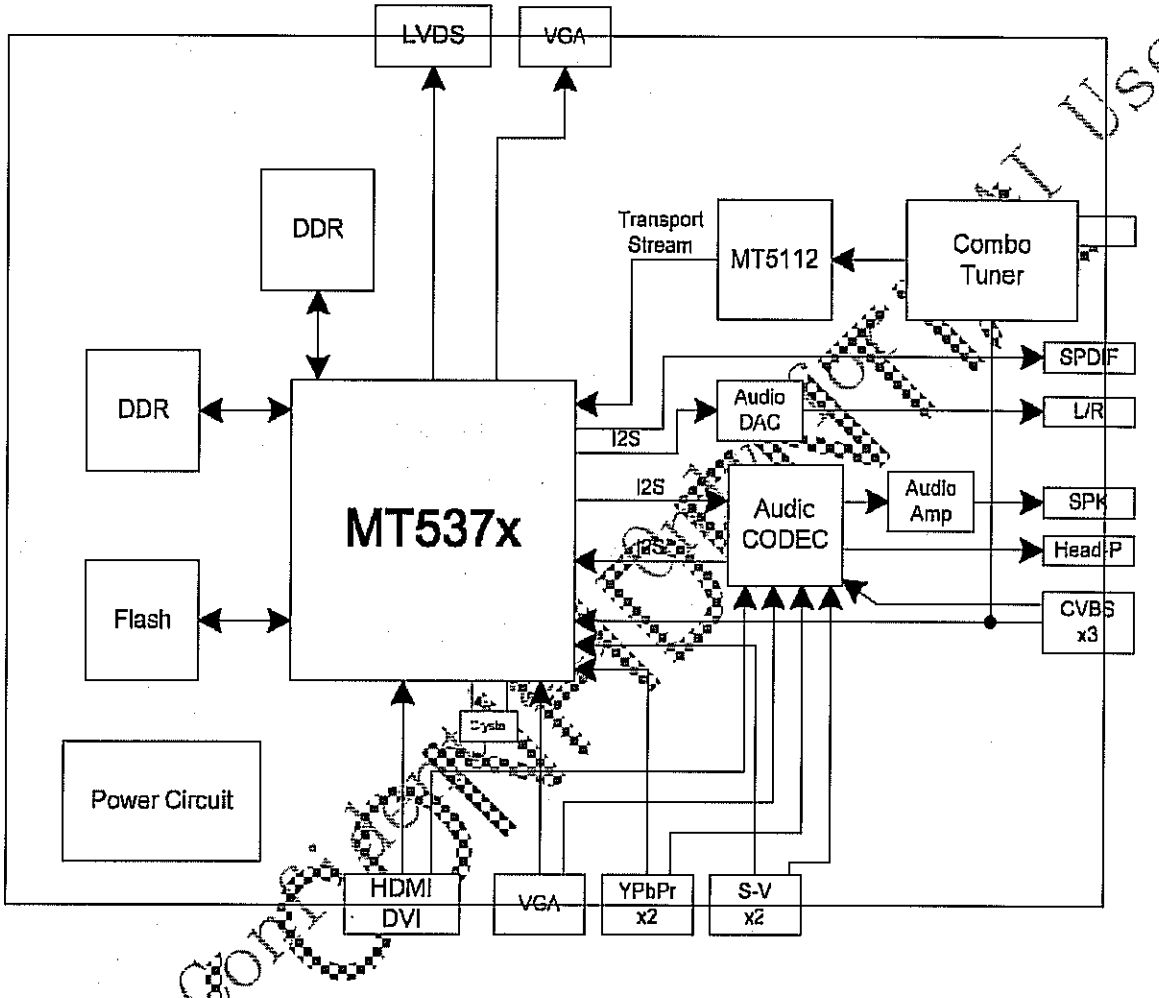
Date	Description	Version
2006/05/18	Initial Version (Draft)	V 0.3
2006/05/27	Updated Power Load Power On/Off Timing	V 0.4
2006/06/06	Update On/Off Timing	V0.5

Specifications are subject to change without notice

2. MT537x Feature

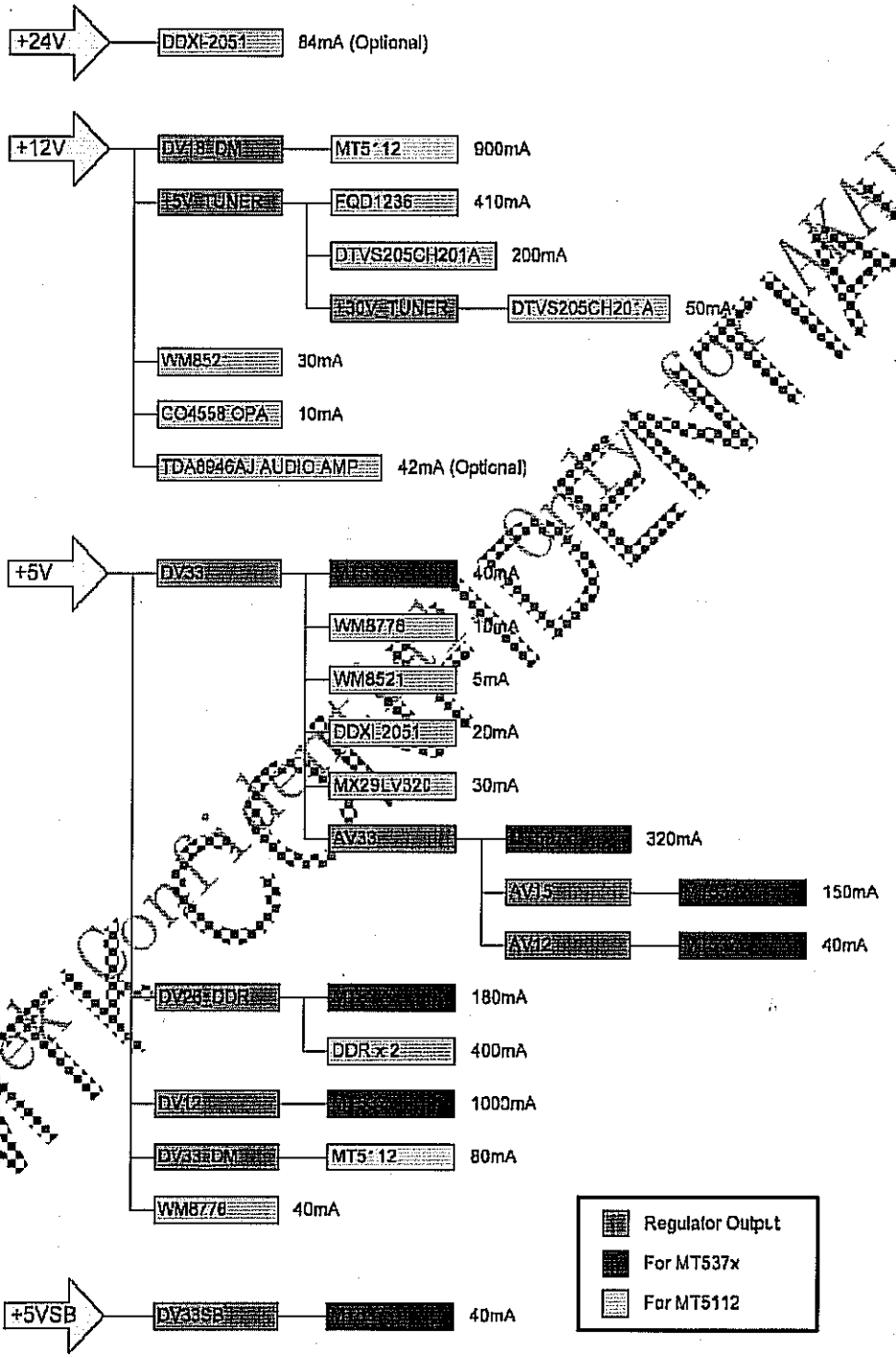
MediaTek MT537x is a highly integrated SOC which include DTV backend decoder and TV controller. MT537x support transport de-multiplexer, MPEG-2 video decoder, AC3 audio decoder, LVDS transmitter, TV decoder. The MT537x enables consumer electronics manufactures to build high quality, feature-rich DTV.
World-Leading Video Technology: MT537x embedded the MDDi deinterlacer to generate very smooth picture quality for motion. 3D comb filter also recovery high detail for still picture. The special color processing technology provided favorite and natural color for TV.
Rich Features for High Value Product: To enrich the features of DTV, MT537x support HDMI receiver, PIP/POP, memory card and DV decoding.
Credible Analog Technology: The MT537x integrated with high speed VGA ADC, high resolution Video/Audio ADC, 90db Audio DAC and 12-bit Video DAC. It will provide very fine quality for TV.

3. DTV System Block (Reference Design)



4. DTV System Power Load (Based on Reference Design)

Specifications are subject to change without notice



Specifications are subject to change without notice

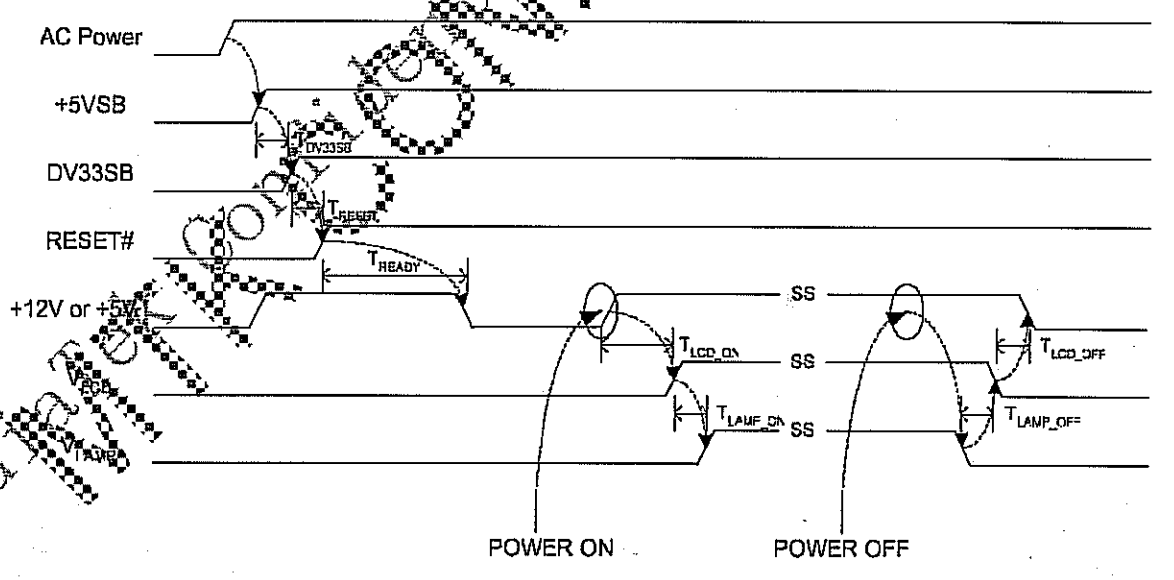
5. MT537x Power Consumption

Under Measurement

Power	Current (mA)	Power Consumption (mW)	PS
DV33	40	132	
AV33	320	1056	
DV26	180	468	
AV15	150	225	
DV12	1000	1200	
AV12	40	48	
DV33SB	40	132	

Note :
Due to We are Under Integration, the Power Consumption Just for Reference. The Power may Increase after Full Function Play.

6. MT537x Power On / Off Timing



Description	Symbol	Min	TPY	Max	Units	PS
DV33SB Power Ready	T_{DV33SB}	0			ms	

Specifications are subject to change without notice

Power-on Reset Period	T_{RESET}	10			ms	
MT537x Boot Ready	T_{READY}		20		ms	
LCD Power On	$T_{LCD\ ON}$				ms	Depend-on Panel
LCD Lamp On	$T_{LAMP\ ON}$				ms	Depend-on Panel
LCD Lamp Off	$T_{LAMP\ OFF}$				ms	Depend-on Panel
LCD Power Off	$T_{LCD\ OFF}$				ms	Depend-on Panel

7. MT537x Diagnostic Program CLI Commands

Under Development

- cd – change current directory
  ex. cd.av – change the directory to AV directory
- do – repeat command
  do "number of times"
  ex. do
- read (r) – memory read
  r "address" "number of bytes"
  ex. r 0x2000d068 8 ← read 8 bytes data from 0x2000d068 address
- write (w) – memory write
  w "address" "data"
  ex. w 0x2000d068 0x12345678 ← write 0x12345678 data to 0x2000d068 address
- basic (b) – basic command
  - stop - stop RS232 transparent mode (set to normal mode)
    ex. b.stop ← set RS232 to normal mode
  - sv – system mode detection
    ex. b.sv ← to detect the system mode
  - reboot – system reboot / restart
    ex. b.reboot ← reboot the system

8. MT537x Debug Flow

Under Development

9. MT537x NOR Flash Supported

Specifications are subject to change without notice

Brand	IC Order Number	Size	Description
MXIC	MX29LV320ABTC-70	32MBits	Under Testing
MXIC	MX29LV320ABTC-90	32MBits	Under Testing
MXIC	MX29LV320ATTC-70	32MBits	Under Testing
MXIC	MX29LV320ATTC-90	32MBits	Under Testing
MXIC	MX29LV320BBTC-70	32MBits	Under Testing
MXIC	MX29LV320BBTC-90	32MBits	Under Testing
MXIC	MX29LV320BTTC-70	32MBits	Under Testing
MXIC	MX29LV320BTTC-90	32MBits	Under Testing
MXIC	MX29LV320BTC-70	32MBits	Under Testing
MXIC	MX29LV320BTC-90	32MBits	Under Testing
MXIC	MX29LV320TTC-70	32MBits	Under Testing
MXIC	MX29LV320TTC-90	32MBits	Under Testing
Winbond	W19B320ABT7H	32MBits	Under Testing
ST	M29W320DT-90	32MBits	Under Testing
ST	M29W320DT-70	32MBits	Under Testing
ST	M29W320DB-70	32MBits	Under Testing
Spansion	S29GL032-90T	32MBits	Under Testing

10. MT537x DDR/2 Supported

Brand	IC Order Number	DDR Type	Description
Nanya	NT5DS32M16BT-5T	DDR	32Mx16, Under Testing
ProMOS	V58C2512164SB5	DDR	32Mx16, Under Testing
Infineon	HYB25DC512160CE–5	DDR	32Mx16, Under Testing
Hynix	HY5DU121622ALT-D43	DDR	32Mx16, Under Testing
MIRA	P2S12D40CTP-G5	DDR	32Mx16, Under Testing
Micron	MT46V32M16TG-5B	DDR	32Mx16, Under Testing
PSC	A2S56D40CTP-G5	DDR	16Mx16, Under Testing
Nanya	NT5DS16M16CS-5T	DDR	16Mx16, Under Testing
ProMOS	V58C2256164SCI5	DDR	16Mx16, Under Testing
Hynix	HY5DU561622CT-5	DDR	16Mx16, Under Testing

Specifications are subject to change without notice

ELPIDA	DD2516AKTA-6B-E	DDR	16Mx16, Under Testing
Infineon	HYB25DC256160CE-5	DDR	16Mx16, Under Testing
MIRA	P2S56D40CTP-G5	DDR	16Mx16, Under Testing
Micron	MT46V16M16TG-5B	DDR	16Mx16, Under Testing
Samsung	K4D551638F-LC50	GDDR	16Mx16, Under Testing
PSC	A3R12E4FDF-G6EA	DDR2	32Mx16, Under Testing
Infinion	HYB18TC512160AF-3S	DDR2	32Mx16, Under Testing
ProMOS	*V59C1512164QA*-3	DDR2	32Mx16, Under Testing
Nanya	NT5TU32M16AG-3C	DDR2	32Mx16, Under Testing
Hynix	HY5PS121621LF-Y5	DDR2	32Mx16, Under Testing
Micron	MT47H32M16-3	DDR2	32Mx16, Under Testing
Infinion	HYB18TC256160AF-3S	DDR2	16Mx16, Under Testing
Hynix	HY5PS561621LF-Y5	DDR2	16Mx16, Under Testing
Micron	MT47H16M16-3	DDR2	16Mx16, Under Testing

11. MT537x PCB Layout Guidelines

- 4-layer PCB Design (TOP / GND / POWER / BOTTOM)
- Power Arrangement
  1. DV33 : Supply to MT537x Digital and Peripheral
  2. AV33 : Supply to MT537x Analog
  3. DV25/DV18 : Supply to MT537x and DDR/2
  4. AV15 : Supply to MT537x Video Front-end 1 (YPbPr/RGB)
  5. AV15_DAC : Supply to MT537x Video DAC
  6. DV12 : Supply to MT537x Digital
  7. AV12 : Supply to MT537x Analog
- Power Plane
  1. The Power has High Priority in Layer 3
  2. If There are No Enough Plane in Layer 3, the Power Line Should be Routed Wider (Component Side Has High Priority)
  3. Be Care the Power Return Path, Especially for Large Power
  4. The Switching Power Should leave alone the Analog Portion
- Ground Plane
  1. In General, We Use Only One Ground (Don't Divided) in Layer 2
  2. You May Have Independent Ground if There are Large Power Consumption in Your Design, for Example - Digital Audio AMP. But You Should Note That the

Specifications are subject to change without notice

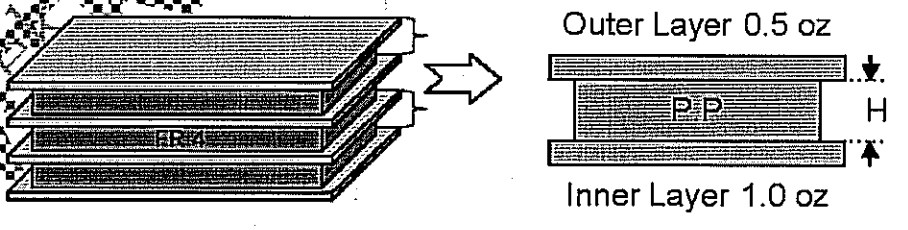
Signal Return Path
3. Please Flush the Copper both in Component and Solder Sides

- The Bypass Cap. Should be Located as Close to IC's Power Pin as Possible
- The VCXO or Crystal Should be Located as Close to IC as Possible
- The Video Termination Resistor Should be Closed to Connector
- The Video AC-couple Cap. Should be Closed to MT537x
- Video Signal YPbPr and RGB Don't Cross with Other Signal (Must)
- Video Signal CVBS and S-Video Don't Cross with Other Signal as Possible. If Need, Please Add Ground Shielding (Guard Trace) on the Side of the Video
- Audio Signal (Analog) Don't Cross with Other Signal as Possible. If Need, Please Add Ground Shielding (Guard Trace) on the Side of the Audio
- To Avoid Routing any Traces on the Ground or Power Plane
- Digital Signal Width Please Use 6 mil
- DDR/2 Layout – Please Follow the Layout Guide Described Below or Copy from MTK's Library to Speed-up the Design Time
  If You had Re-layout the DDR/2, Please Provide the Layout File for DDR/2 SI Simulation (Familiar with PowerPCB Format)
- HDMI / LVDS Layout – Please Follow the Layout Guide Described Below

12. MT537x DDR/2 Layout Guide

12.1 4 Layer PCB Layout Constraints

12.1.1 Board Stack-up



PCB Stackup – 4 Layers

Specifications are subject to change without notice

The outer layers of the PCB were designated to the mainly signal routings by default, and normally were chosen to have the 0.5 oz Cu foil with plated 0.5 oz copper, and the inner layers was designated to be 1.0 oz at the PCB manufacturing step.

The dielectrics between conductors were as the isolators, which were used to separate the conductors. By the micro-strip line architecture of system memory signals, the target impedance was desired to have 55Ω +/- 10%. Please refer to the table below for your PCB design and recommendation. The default design was 6 mil trace width with 4.5 mil height dielectrics.

4 Layer PCB Stack-up Configurations

PCB Parameter			
Trace Width (mil)	H (mil)	Target Impedance (Ω)	Tolerance
5	4.5	56	10%

Please request the PCB manufactory to follow the FR4 stack-up as below

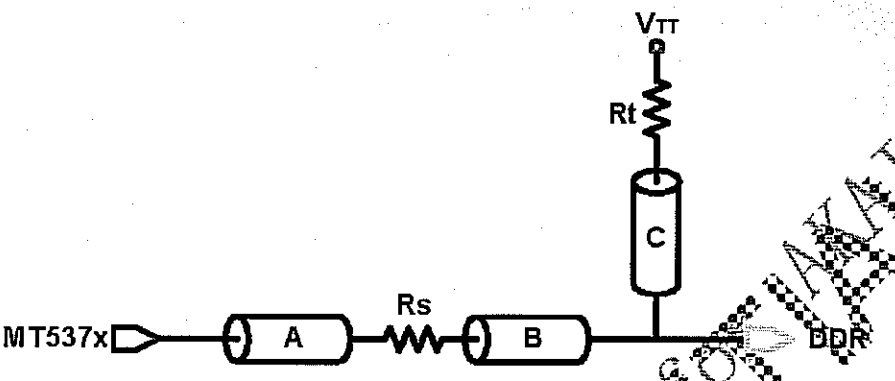
Description	Material	Height (mil)	PS
Conductor		0.5 oz	
Medium	☐ No Assigned ☒ Assigned	4.5	2116
Conductor		1 oz	
Medium		47.6	
Conductor		1 oz	
Medium		4.5	
Conductor		0.5 oz	

12.2 System DDR Memory Solution Space

Refer to the diagrams below to the topologies of the DDR signals, and the actual dimension specifications were listed of the tables

12.2.1 DDR Signal Topology – 1 (DS / DQS / DQM)

Specifications are subject to change without notice



DDR Signal Topology - 1

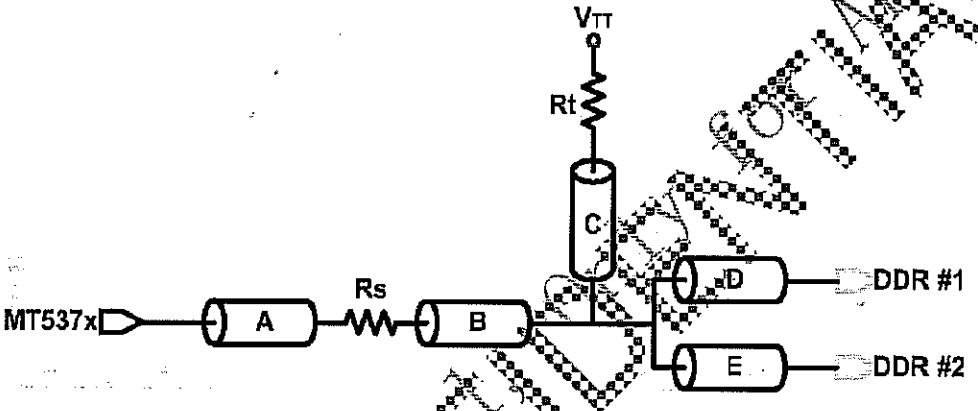
Signal			DQ	DQS	DQM
Trace (mil)		Width (W)	5	5	5
		Spacing	8 or Above	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2	0.2	0.2
		Max.	1	1	1
	B	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	C	Min.	0.1	0.1	0.1
		Max.	0.5	0.5	0.5
	A+B	Min.	0.4	0.4	0.4
		Max.	2	2	2
Rs (Ω)			47	47	47
Rt (Ω)			75	75	75

Note :

1. Keep the difference of the trace length of the same data signal groups within about 200 mils as possible.
2. Keep the difference of the data signal groups within 200 mils as possible (The longest signal trace to the shortest signal trace).
3. Placing the damping resistor close to the MT537x.
4. Placing the termination resistor close to the memory as possible.
5. Put an integrated plane as the return path to the signals beneath the data signals.
6. When the signal need to change layers, and the reference paths beneath

the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.2.2 DDR Signal Topology – 2 (Address and Command)



DDR Signal Topology - 2

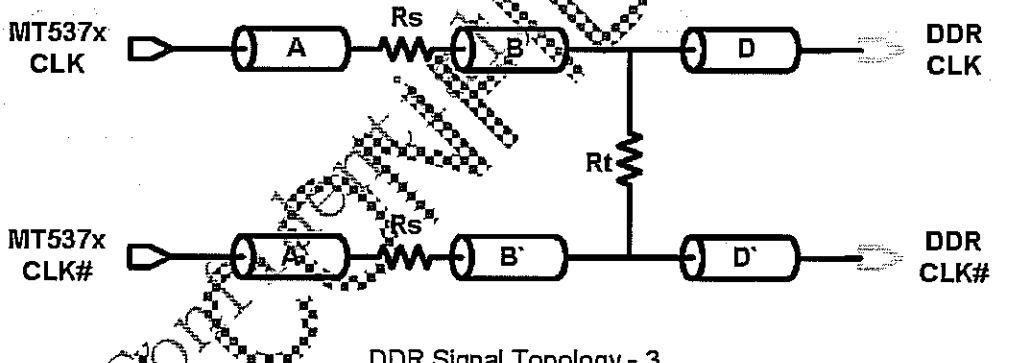
Signal			RA / BA	CS# / CAS# / RAS# / WE#	CKE
Trace (mil)		Width (W)	5	5	5
		Spacing	8 or Above	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	B	Min.	0.2	0.2	0.2
		Max.	2	2	2
	C	Min.	0	0	0
		Max.	0.5	0.5	0.5
	D / E	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	A+B+D (or E)	Min.	0.6	0.6	0.6
		Max.	4.2	4.2	4.2
Rs (Ω)			22	22	22
Rt (Ω)			75	75	75

Specifications are subject to change without notice

Note :

1. Keep the difference of the branches' length (D / E) of the dual loads signal within 100 mils.
2. Placing the damping resistor close to the MT537x.
3. Put the termination resistor close to the crossing point of the branches.
4. Reserving more spacing to the periodic signal (as clock) if signal was critical and there weren't the guard traces.
5. Put an integrated plane as the return path to the signals beneath the address / command signals.
6. When the signal need to change layers, and the reference paths beneath the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.2.3 DDR Signal Topology – 3 (Clock Pair)



DDR Signal Topology - 3

Signal			CLK / CLK#
Trace (mil)		Width	5
		Spacing	8 or Above
Trace Length (inch)	A	Min.	0.2
		Max.	1
	B	Min.	0.2
		Max.	1
	D	Min.	0.2
		Max.	1.2
	A+B+D	Min.	0.6

Specifications are subject to change without notice

		Max.	2.6
Rs (Ω)			47
Rt (Ω)			100

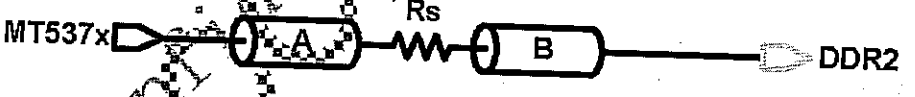
Note :

1. The trace length of A / A`, B / B`, D / D` should be as equal as possible.
2. Keep the trace difference between CLK / CLK# in +/- 100 mils.
3. Keep the trace difference between DQ / DQS / DQM and CLK in +/- 200 mils.
4. Keep the trace difference between RA / BA / CS# / CAS# / RAS# / WE# / CKE and CLK in +/- 1000 mils.

12.3 System DDR2 Memory Solution Space

Refer to the diagrams below to the topologies of the DDR2 signals, and the actual dimension specifications were listed of the tables.

12.3.1 DDR2 Signal Topology – 1 (DQ and DQM)



DDR2 Signal Topology - 1

Signal			DQ	DQM
Trace (mil)		Width (W)	5	5
		Spacing	8 or Above	8 or Above
Lengt	A	Min.	0.2	0.2
		Max.	1	1
	B	Min.	0.2	0.2

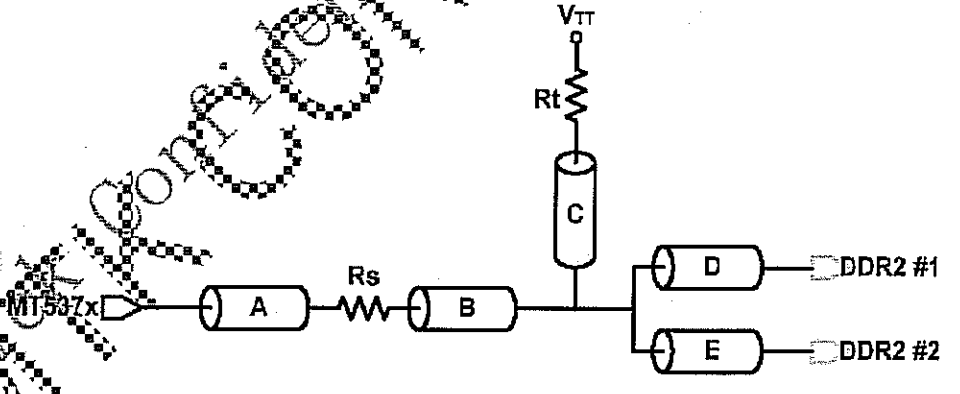
Specifications are subject to change without notice

		Max.	1.2	1.2
	A+B	Min.	0.4	0.4
		Max.	2	2
Rs (Ω)			22	22

Note :

1. Keep the difference of the trace length of the same data signal groups within about 200 mils as possible.
2. Keep the difference of the data signal groups within 200 mils as possible (The longest signal trace to the shortest signal trace).
3. Placing the damping resistor close to the MT537x as possible.
4. Placing the termination resistor close to the memory as possible.
5. Put an integrated plane as the return path to the signals beneath the data signals.
6. When the signal need to change layers and the reference paths beneath the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.3.2 DDR2 Signal Topology – 2 (Address and Command)



DDR2 Signal Topology - 2

Signal		RA / BA	CS# / CAS# / RAS# / WE#	CKE
Trace (mil)	Width (W)	5	5	5

Specifications are subject to change without notice

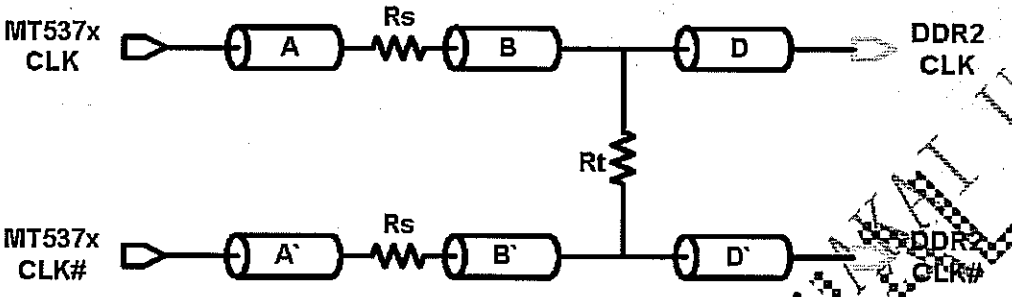
		Spacing	8 or Above	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	B	Min.	0.2	0.2	0.2
		Max.	2	2	2
	C	Min.	0	0	0
		Max.	0.5	0.5	0.5
	D / E	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	A+B+D (or E)	Min.	0.6	0.6	0.6
		Max.	4.2	4.2	4.2
Rs (Ω)			22	22	22
Rt (Ω)			75	75	75

Note :

1. Keep the difference of the branches' length (D / E) of the dual loads signal within 100 mils.
2. Placing the damping resistor close to the MT537x.
3. Put the termination resistor close to the crossing point of the branches.
4. Reserving more spacing to the periodic signal (as clock) if signal was critical and there weren't the guard traces.
5. Put an integrated plane as the return path to the signals beneath the address / command signals.
6. When the signal need to change layers, and the reference paths beneath the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.3.3 DDR2 Signal Topology – 3 (Clock and DQS)

Specifications are subject to change without notice



DDR2 Signal Topology - 3

Signal			CLK / CLK#	DQS / DQS#
Trace (mil)		Width (W)	5	5
		Spacing	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2	0.2
		Max.	1	1
	B	Min.	0.2	0.2
		Max.	1	1
	D	Min.	0.1	NS
		Max.	1.2	NS
	A+B+D	Min.	0.6	0.4
		Max.	2.6	2
Rs (Ω)			22	22
Rt (Ω)			100	NS

Note :

1. The trace length of A / A`, B / B`, D / D` should be as equal as possible.
2. Keep the trace difference between CLK / CLK# in +/- 100 mils.
3. Keep the trace difference between DQ / DQS / DQM and CLK in +/- 200 mils.
4. Keep the trace difference between RA / BA / CS# / CAS# / RAS# / WE# / CKE and CLK in +/- 1000 mils.

13. MT537x HDMI / LVDS Layout Guide

13.1 HDMI / LVDS Signal PCB Layout Guideline

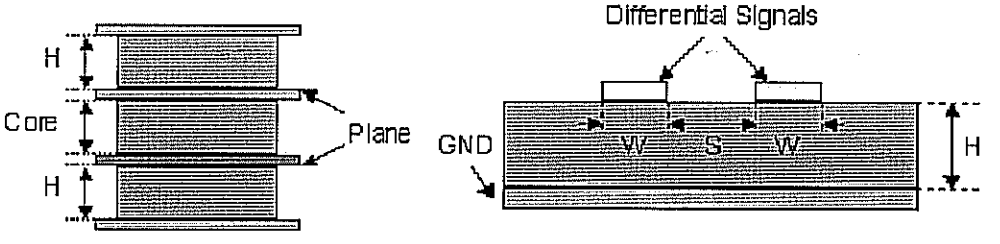
Specifications are subject to change without notice

For the other applications of the high-speed signal PCB design, below illustrated the topologies and constraints of the HDMI / LVDS or other differential signals that were achieved to the electrical requirements. Also refer to the form to the detail recommendations.

13.2 Multi-Layer PCB Design

By the default multi-layers PCB architecture, the inner layers were assigned to be the reference plane to the signals. For the signal integrity issues, the integrate plane would held to hold a good signal qualities when signal were proceeding on the signal traces. Refer to the below shown the stack up and the topology of the differential signals of the 4-layer PCB where the signals were routed of the outer layers.

13.2.1 Signals without Guard Traces



HDMI / LVDS Signal Topology - 4 Layer

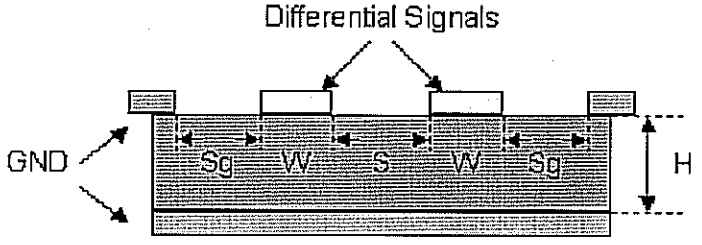
Variable	Nominal (mil)	Tolerance	Min. (mil)	Max. (mil)
Trace High (H)	4.5 (2116)			
Trace Width (W)	5	+/- 1 mil	4	6
Spacing (S)	8 (mil)	+/- 1 mil	9	7
Single Ended Trace Impedance	56Ω		61.6Ω	52.6Ω
Differential Trace Impedance	98Ω		109Ω	89.9Ω
Reference Plane	Ground	Ground	Ground	Ground

13.2.2 Signals with Guard Traces

The other application was used the coplanar ground copper and surrounded the

Specifications are subject to change without notice

signals to achieve the noise shielding purpose. The figure shows the signal topology.

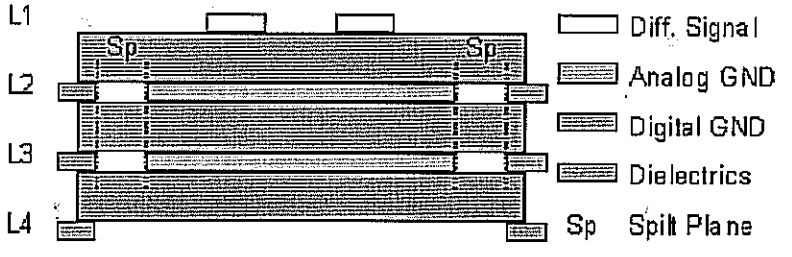


Differential Signal with Guard Trace

Variable	Nominal (mil)	Tolerance	Min. (mil)	Max. (mil)
Trace High (H)	4.5 (2116)			
Trace Width (W)	5	+/- 1 mil	4	6
Spacing (S)	8 (mil)	+/- 1 mil	9	7
Spacing to GND(Sg)	8 (mil)	+/- 1 mil	9	7
Single Ended Trace Impedance	55Ω		60Ω	50.5Ω
Differential Trace Impedance	97Ω		107Ω	87Ω
Reference Plane	Ground	Ground	Ground	Ground

Note:

1. Keeping the spacing to the other signals as far as possible.
2. Keeping the spacing to different ground planes (Sp) more than 30 mils as possible as the below.



Cross-Section of Plane Designated

Specifications are subject to change without notice

14. MT537x BGA Soldering Information

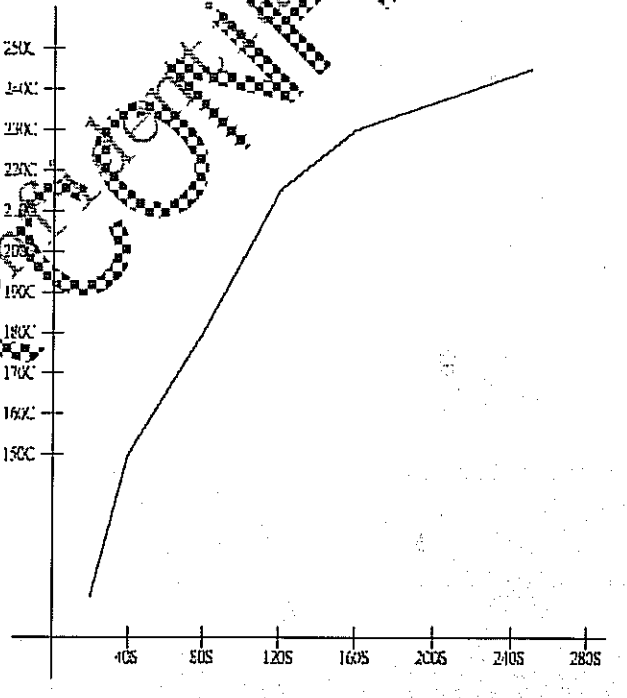
14.1 MT537xAG is Lead-Free Process

Element :

1. Sn : 95.5 %
2. Ag : 4 %
3. Cu : 0.3 %
4. Fusion Point : 228 °C.

14.2 Soldering Control (for Reference Only)

1. 150 °C : 40 Sec
2. 180 °C : 40 Sec
3. 215 °C : 40 Sec
4. 230 °C : 40 Sec
5. 245 °C : 90 Sec
6. 245 °C : 30 Sec



Specifications are subject to change without notice

15. US Terrestrial TV Channel Frequencies

US Terrestrial TV Channel Frequencies					
Channel	TV Video Freq (MHz)	ATSC Center Freq (MHz)	Channel	Video Freq (MHz)	ATSC Center Freq (MHz)
2	55.25	57	36	603.25	605
3	61.25	63	37	609.25	611
4	67.25	69	38	615.25	617
5	77.25	79	39	621.25	623
6	83.25	85	40	627.25	629
7	175.25	177	41	633.25	635
8	181.25	183	42	639.25	641
9	187.25	189	43	645.25	647
10	193.25	195	44	651.25	653
11	199.25	201	45	657.25	659
12	205.25	207	46	663.25	665
13	211.25	213	47	669.25	671
14	471.25	473	48	675.25	677
15	477.25	479	49	681.25	683
16	483.25	485	50	687.25	689
17	489.25	491	51	693.25	695
18	495.25	497	52	699.25	701
19	501.25	503	53	705.25	707
20	507.25	509	54	711.25	713
21	513.25	515	55	717.25	719
22	519.25	521	56	723.25	725
23	525.25	527	57	729.25	731
24	531.25	533	58	735.25	737
25	537.25	539	59	741.25	743
26	543.25	545	60	747.25	749
27	549.25	551	61	753.25	755

28	555.25	557	62	759.25	761
29	561.25	563	63	765.25	767
30	567.25	569	64	771.25	773
31	573.25	575	65	777.25	779
32	579.25	581	66	783.25	785
33	585.25	587	67	789.25	791
34	591.25	593	68	795.25	797
35	597.25	599	69	801.25	803

16. US Cable TV Channel Frequencies

16.1 Standard TV Channel

US Cable TV STD Channel Frequencies					
Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)	Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)
2	55.25	57	64	463.25	465
3	61.25	63	65	469.25	471
4	67.25	69	66	475.25	477
1	–	–	67	481.25	483
5	77.25	79	68	487.25	489
6	83.25	85	69	493.25	495
95	91.25	93	70	499.25	501
96	97.25	99	71	505.25	507
97	103.25	105	72	511.25	513
98	109.25	111	73	517.25	519
99	115.25	117	74	523.25	525
14	121.25	123	75	529.25	531
15	127.25	129	76	535.25	537
16	133.25	135	77	541.25	543
17	139.25	141	78	547.25	549
18	145.25	147	79	553.25	555
19	151.25	153	80	559.25	561

Specifications are subject to change without notice

20	157.25	159	81	565.25	567
21	163.25	165	82	571.25	573
22	169.25	171	83	577.25	579
7	175.25	177	84	583.25	585
8	181.25	183	85	589.25	591
9	187.25	189	86	595.25	597
10	193.25	195	87	601.25	603
11	199.25	201	88	607.25	609
12	205.25	207	89	613.25	615
13	211.25	213	90	619.25	621
23	217.25	219	91	625.25	627
24	223.25	225	92	631.25	633
25	229.25	231	93	637.25	639
26	235.25	237	94	643.25	645
27	241.25	243	100	649.25	651
28	247.25	249	101	655.25	657
29	253.25	255	102	661.25	663
30	259.25	261	103	667.25	669
31	265.25	267	104	673.25	675
32	271.25	273	105	679.25	681
33	277.25	279	106	685.25	687
34	283.25	285	107	691.25	693
35	289.25	291	108	697.25	699
36	295.25	297	109	703.25	705
37	301.25	303	110	709.25	711
38	307.25	309	111	715.25	717
39	313.25	315	112	721.25	723
40	319.25	321	113	727.25	729
41	325.25	327	114	733.25	735
42	331.25	333	115	739.25	741
43	337.25	339	116	745.25	747
44	343.25	345	117	751.25	753
45	349.25	351	118	757.25	759
46	355.25	357	119	763.25	765
47	361.25	363	120	769.25	771
48	367.25	369	121	775.25	777
49	373.25	375	122	781.25	783

Specifications are subject to change without notice

50	379.25	381	123	787.25	789
51	385.25	387	124	793.25	795
52	391.25	393	125	799.25	801
53	397.25	399	126	805.25	807
54	403.25	405	127	811.25	813
55	409.25	411	128	817.25	819
56	415.25	417	129	823.25	825
57	421.25	423	130	829.25	831
58	427.25	429	131	835.25	837
59	433.25	435	132	841.25	843
60	439.25	441	133	847.25	849
61	445.25	447	134	853.25	855
62	451.25	453	135	859.25	861
63	457.25	459			

16.2 IRC TV Channel

US Cable TV IRC Channel Frequencies					
Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)	Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)
2	55.25	57	64	463.25	465
3	61.25	63	65	469.25	471
4	67.25	69	66	475.25	477
1	73.25	75	67	481.25	483
5	79.25	81	68	487.25	489
6	85.25	87	69	493.25	495
95	91.25	93	70	499.25	501
96	97.25	99	71	505.25	507
97	103.25	105	72	511.25	513
98	–	–	73	517.25	519
99	–	–	74	523.25	525
14	121.15	122.9	75	529.25	531

Specifications are subject to change without notice

15	127.15	128.9	76	535.25	537
16	133.15	134.9	77	541.25	543
17	139.15	140.9	78	547.25	549
18	145.15	146.9	79	553.25	555
19	151.15	152.9	80	559.25	561
20	157.15	158.9	81	565.25	567
21	163.15	164.9	82	571.25	573
22	169.15	170.9	83	577.25	579
7	175.25	177	84	583.25	585
8	181.25	183	85	589.25	591
9	187.25	189	86	595.25	597
10	193.25	195	87	601.25	603
11	199.25	201	88	607.25	609
12	205.25	207	89	613.25	615
13	211.25	213	90	619.25	621
23	217.25	219	91	625.25	627
24	223.25	225	92	631.25	633
25	229.25	234	93	637.25	639
26	235.25	237	94	643.25	645
27	241.25	243	100	649.25	651
28	247.25	249	101	655.25	657
29	253.25	255	102	661.25	663
30	259.25	261	103	667.25	669
31	265.25	267	104	673.25	675
32	271.25	273	105	679.25	681
33	277.25	279	106	685.25	687
34	283.25	285	107	691.25	693
35	289.25	291	108	697.25	699
36	295.25	297	109	703.25	705
37	301.25	303	110	709.25	711
38	307.25	309	111	715.25	717
39	313.25	315	112	721.25	723
40	319.25	321	113	727.25	729
41	325.25	327	114	733.25	735

Specifications are subject to change without notice

42	--	--	115	739.25	741
43	337.25	339	116	745.25	747
44	343.25	345	117	751.25	753
45	349.25	351	118	757.25	759
46	355.25	357	119	763.25	765
47	361.25	363	120	769.25	771
48	367.25	369	121	775.25	777
49	373.25	375	122	781.25	783
50	379.25	381	123	787.25	789
51	385.25	387	124	793.25	795
52	391.25	393	125	799.25	801
53	397.25	399	126	805.25	807
54	403.25	405	127	811.25	813
55	409.25	411	128	817.25	819
56	415.25	417	129	823.25	825
57	421.25	423	130	829.25	831
58	427.25	429	131	835.25	837
59	433.25	435	132	841.25	843
60	439.25	441	133	847.25	849
61	445.25	447	134	853.25	855
62	451.25	453	135	859.25	861
63	457.25	459			

16.3 HRC TV Channel

US Cable TV HRC Channel Frequencies					
Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)	Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)
2	54	55.75	64	462	463.75
3	60	61.75	65	468	469.75

Specifications are subject to change without notice

4	66	67.75	66	474	475.75
1	72	73.75	67	480	481.75
5	78	79.75	68	486	487.75
6	84	85.75	69	492	493.75
95	90	91.75	70	498	499.75
96	96	97.75	71	504	505.75
97	102	103.75	72	510	511.75
98	–	–	73	516	517.75
99	–	–	74	522	523.75
14	120	121.75	75	528	529.75
15	126	127.75	76	534	535.75
16	132	133.75	77	540	541.75
17	138	139.75	78	546	547.75
18	144	145.75	79	552	553.75
19	150	151.75	80	558	559.75
20	156	157.75	81	564	565.75
21	162	163.75	82	570	571.75
22	168	169.75	83	576	577.75
7	174	175.75	84	582	583.75
8	180	181.75	85	588	589.75
9	186	187.75	86	594	595.75
10	192	193.75	87	600	601.75
11	198	199.75	88	606	607.75
12	204	205.75	89	612	613.75
13	210	211.75	90	618	619.75
23	216	217.75	91	624	625.75
24	222	223.75	92	630	631.75
25	228	229.75	93	636	637.75
26	234	235.75	94	642	643.75
27	240	241.75	100	648	649.75
28	246	247.75	101	654	655.75
29	252	253.75	102	660	661.75
30	258	259.75	103	666	667.75
31	264	265.75	104	672	673.75

Specifications are subject to change without notice

32	270	271.75	105	678	679.75
33	276	277.75	106	684	685.75
34	282	283.75	107	690	691.75
35	288	289.75	108	696	697.75
36	294	295.75	109	702	703.75
37	300	301.75	110	708	709.75
38	306	307.75	111	714	715.75
39	312	313.75	112	720	721.75
40	318	319.75	113	726	727.75
41	324	325.75	114	732	733.75
42	330	331.75	115	738	739.75
43	336	337.75	116	744	745.75
44	342	343.75	117	750	751.75
45	348	349.75	118	756	757.75
46	354	355.75	119	762	763.75
47	360	361.75	120	768	769.75
48	366	367.75	121	774	775.75
49	372	373.75	122	780	781.75
50	378	379.75	123	786	787.75
51	384	385.75	124	792	793.75
52	390	391.75	125	798	799.75
53	396	397.75	126	804	805.75
54	402	403.75	127	810	811.75
55	408	409.75	128	816	817.75
56	414	415.75	129	822	823.75
57	420	421.75	130	828	829.75
58	426	427.75	131	834	835.75
59	432	433.75	132	840	841.75
60	438	439.75	133	846	847.75
61	444	445.75	134	852	853.75
62	450	451.75	135	858	859.75
63	456	457.75			

MT5112BD
Preliminary Datasheet

- FEATURES
- GENERAL DESCRIPTION
- FUNCTIONAL BLOCK DIAGRAM
- PIN ASSIGNMENT
- PIN DESCRIPTION
- TIMING INFORMATION
- ELECTRICAL CHARACTERISTICS
- OUTLINE DIMENSION & TOP MARKING

FEATURES

- Compliant with ATSC digital television standard
- Supports SCTE DVS-031 and ITU J.83 Annex B digital CATV standard
- Accepts direct IF (44 MHz or 43.75MHz) and low IF (5.38MHz)
- Differential IF input with programmable input signal level: 0.5Vpp to 2Vpp
- NTSC interference rejection capability
- Compensate echo up to -35 to +60*us* range for terrestrial HDTV reception
- Pass all Brazil fading channel ensembles
- Meet all ATSC/A74 requirement
- On-chip programmable gain amplifier
- 25MHz crystal for clock generation
- Excellent adjacent and co-channel rejection capability, only single SAW is required
- Full-digital timing recovery, no VCXO is required
- Full-digital frequency offset recovery with wide acquisition range ±1MHz for ATSC and ±250kHz for CATV reception
- Dual digital AGC controls for IF and RF respectively
- MPEG-2 transport stream output in parallel or serial format
- On-chip error rate estimators for TS packets, TCM decoder, and equalizer
- EIA/CEA-909 antenna interface, both mode A and mode B are supported
- Controlled by I^2C interface
- Supports sleep mode to save power consumption
- Core power supply: 1.8V, peripheral power supply: 3.3V
- 100-TQFP with lead free package

GENERAL DESCRIPTION

The MT5112BD is a highly integrated single-chip for digital terrestrial HDTV and digital cable TV demodulation. The chip is designed specifically for the digital terrestrial HDTV and CATV receivers, and is fully compliant with ATSC A/53, SCTE DVS-031, and ITU J.83 Annex B standards.

8-VSB and Clear-QAM Reception

MT5112BD contains a 10-bit A/D converter, an 8-VSB/QAM demodulator, followed by a trellis-coded modulation (TCM) decoder and a Reed-Solomon forward error correction (FEC) decoder. Moreover, an embedded 8-bit microprocessor intelligently handles the acquisition and tracking to ensure the best receiving performance under various channel conditions. The microprocessor communicates with the external host controller via an I^2C-compatible interface, and also provides direct control to the RF tuner via another I^2C-compatible interface.

MT5112BD accepts the tuner IF output centered at 44MHz or 43.75MHz, or the low IF signals from a down-converter. With good adjacent channel immunity, additional IF SAW filters for adjacent channel rejection can be saved. An on-chip programmable gain-controlled amplifier (PGA) is designed to provide extra signal gain when the tuner output level is low. The amplified IF signal is then sample and digitized for further demodulation process.

MT5112BD keeps A/D input power level at a desired level so as to maximize the received SNR. It measures the power level of the digitized samples and provide two signals (both sigma-delta encoded; one delayed and one non-delayed) for front-end gain control purpose. The signals is low-pass filtered before connected to tuner or IF gain stages.

For the 8-VSB reception, the carrier frequency offset is estimated and compensated by a fully digital synchronizer. It also controls the rate conversion in the digital re-sampling device by estimating the sampling frequency offset; hence no external VCXO is required. The digital synchronizer simultaneously offers very wide frequency acquisition range and stable tracking capability. This makes MT5112BD robust

work under severe impairment conditions.

The MT5112BD is equipped with a powerful equalizer for mitigating the multi-path effects due to terrestrial propagation of 8-VSB signals. The delicate equalizer design makes the MT5112BD boast its ability for strong echo cancellation. With this powerful equalizer, the MT5112BD can not only easily pass the tests of A74 equalization mask, ATTC channel ensembles, CRC channel ensembles, but also provide superior capability of live signal receptions.

For cable signal reception, the MT5112BD adopts the fully digital modules for timing and carrier synchronization, with no external VCXO required. Specially designed carrier synchronization module enables the MT5112BD passing the OpenCable ATP burst and phase noise tests, while maintaining excellent reception performance under normal reception conditions.

The MT5112BD also utilizes a powerful equalizer for performing channel equalization in cable environments. The MT5112BD equipped with this powerful equalizer can easily pass the SCTE channel tests and offer stable and excellent live signal receptions.

The following FEC decoder corrects most of the errors by the concatenation of the TCM and Reed-Solomon decoders with an in-between de-interleaver. Specifically for the digital cable TV reception, the MT5112BD first detects and aligns de-puncturing timing of the received sequence before TCM decoding. Besides, two synchronization circuits are each inserted before the de-interleaver and after the Reed-Solomon decoder to automatically delineate the FEC frames and transport stream packets respectively. An on-chip error rate estimator can simultaneously monitor the receiving qualities at the three stages: the equalizer output, the TCM decoder, and the transport stream packets. At the last stage, the MT5112BD incorporates a buffer to smooth out the uneven arrival time of transport stream packets. The chip finally outputs the smoothed decoded MPEG-2 transport stream packets in either the serial or parallel transport stream format.

In addition to the demodulation of HDTV signal, MT5112BD provides the capability to remove narrow-band interference such as the co-channel NTSC signal and CW tones which generally exists in

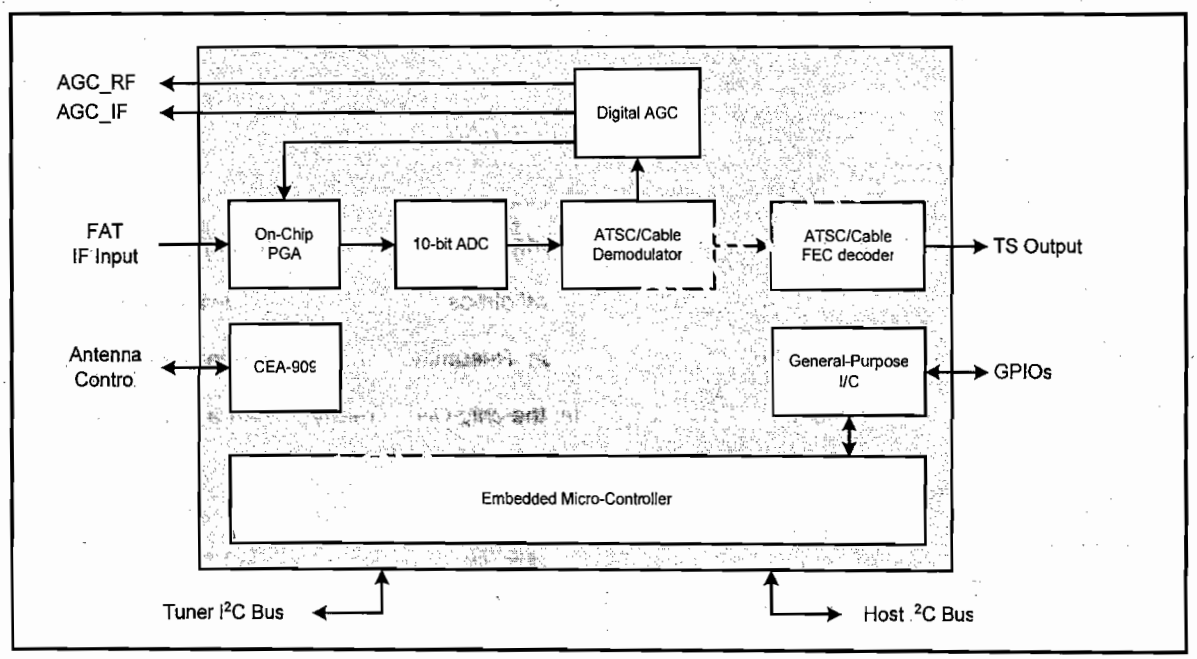
broadcast environment.

To achieve the best reception, an antenna control interface compliant with EIA/CEA-909 is equipped into the MT5112BD to configure the antenna parameters. Both the unidirectional mode A and the bi-directional mode B operation schemes are supported.

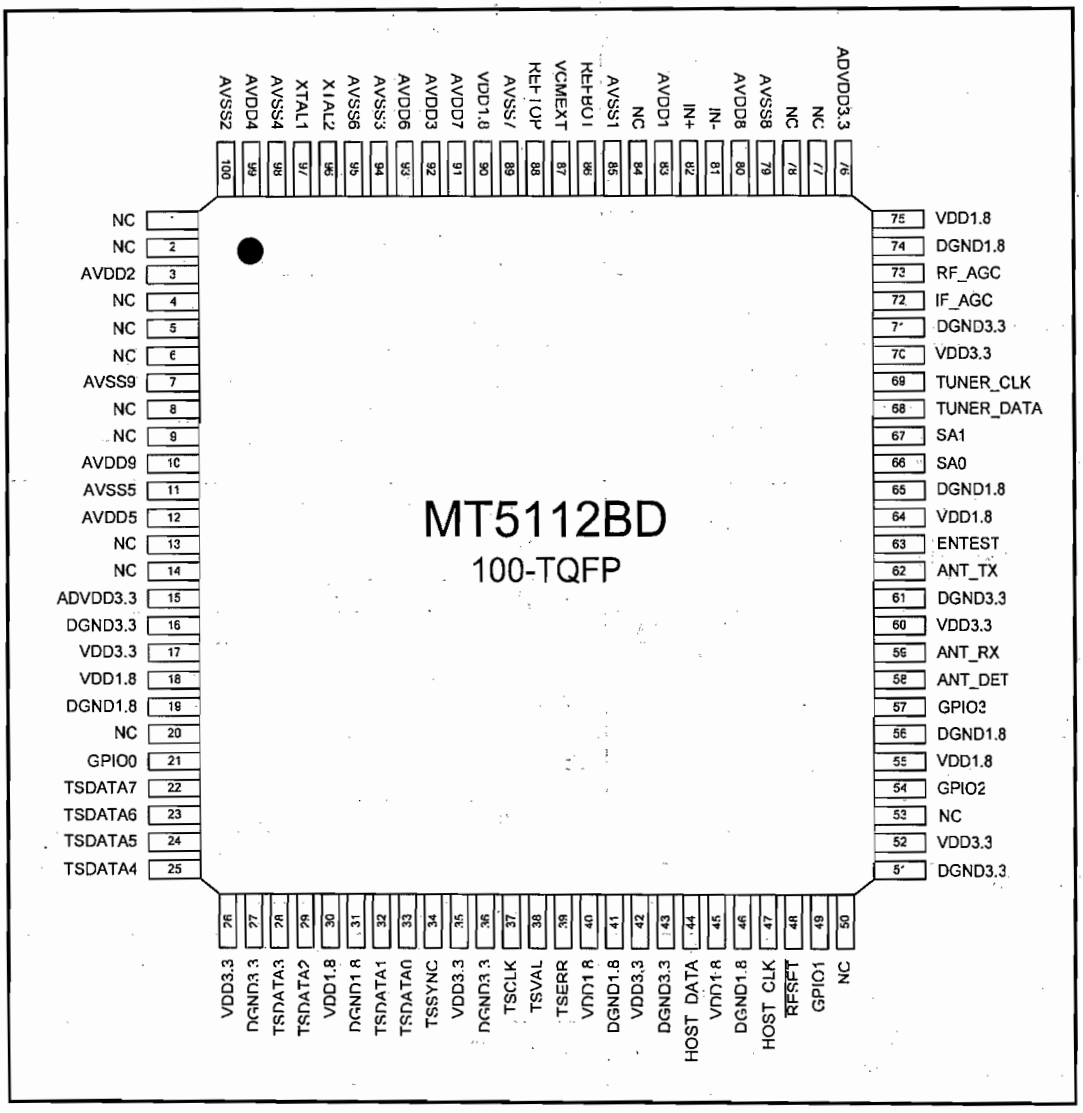
Power Saving Mode

The MT5112BD is designed with efficient mechanisms of power saving. When configured to enter the sleep mode by the system host, it can immediately turn off almost all embedded hardware except the on-chip microprocessor to reduce the power consumption. Resuming from sleep mode is also triggered by the system host. Upon returning to the operation mode, the chip will be ready to start a new acquisition.

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTION

For FAT Applications

Pin Numbers	Symbol	Type	Description
Transport Stream			
22, 23, 24, 25, 28, 29, 32, 33	TSDATA[7:0]	O	TS data output
34	TSSYNC	O	TS packet start signal
38	TSVAL	O	TS output valid signal
37	TSCLK	O	TS output clock
39	TSERR	O	TS packet error indicator
Analog Signal			
82	IN+	I	Analog differential IF input
81	IN-	I	
88	REFTOP	O	ADC reference top voltage. Decouple with a capacitor to AVSS
86	REFBOT	O	ADC reference bottom voltage. Decouple with a capacitor to AVSS
87	VCMEXT	O	ADC common mode voltage
Antenna Interface			
62	ANT_TX	O	CEA-909 antenna control: transmit data
58	ANT_DET	I	CEA-909 antenna control: detection signal
59	ANT_RX	I	CEA-909 antenna control: receive data
Clock Generation			
97	XTAL1	I	25MHz crystal input
96	XTAL2	I	
Control Signals			
47	HOST_CLK	I	Host processor serial clock input, 5 volt compatible
44	HOST_DATA	I/O	Host processor serial data pin, 5 volt compatible
69	TUNER_CLK	O	Tuner serial clock output, 5 volt compatible
68	TUNER_DATA	I/O	Tuner serial data pin, 5 volt compatible
72	IF_AGC	O	IF AGC output
73	RF_AGC	O	RF AGC output
48	RESET	I	Power reset pin, low active
66	SA0	I	Chip slave address selection pin, tie to VDD3.3 or DGND
67	SA1	I	Chip slave address selection pin, tie to VDD3.3 or DGND
Power Supply			
17, 26, 35, 42, 52, 60, 70	VDD3.3	P	Digital power supply, tie to 3.3V
18, 30, 40, 45, 55, 64, 75	VDD1.8	P	Digital power supply, tie to 1.8V
16, 19, 27, 31, 36, 41, 43, 46, 51, 56, 61, 63, 65, 71, 74	DGND	P	Digital ground, tie to digital ground plane
3, 10, 12, 80, 83, 91, 92, 93, 99	AVDD	P	Analog power supply, tie to 3.3V
7, 11, 79, 85, 89, 94, 95, 98, 100	AVSS	P	Analog ground, tie to analog ground plane
15, 76	ADVDD3.3	P	Digital power supply for analog component, tie to 3.3V
90	AVDD1.8	P	Digital power supply for analog component, tie to 1.8V
General-Purpose I/O			
57, 54, 49, 21	GPIO[3:0]	I/O	General-Purpose I/Os

24-bit, 192 KHz. CODEC: 6 Ch DAC, 5 Input Mux Stereo ADC

DESCRIPTION

The CE2836 is a mixed signal CMOS monolithic audio Codec. It contains six multi-bit sigma delta DAC and a stereo ADC with 5 input multiplexer, Ideal for audio playback and recording applications.

The DAC consists of 128-time interpolation filters, 3rd order multi-bit ΣΔ modulators, switch capacitors and analog reconstruction filters. The ΣΔ converter offers superior differential linearity, with minimum distortion due to component mis-match. high tolerance to clock jitter. Additionally it includes separated digital volume control for each channel.

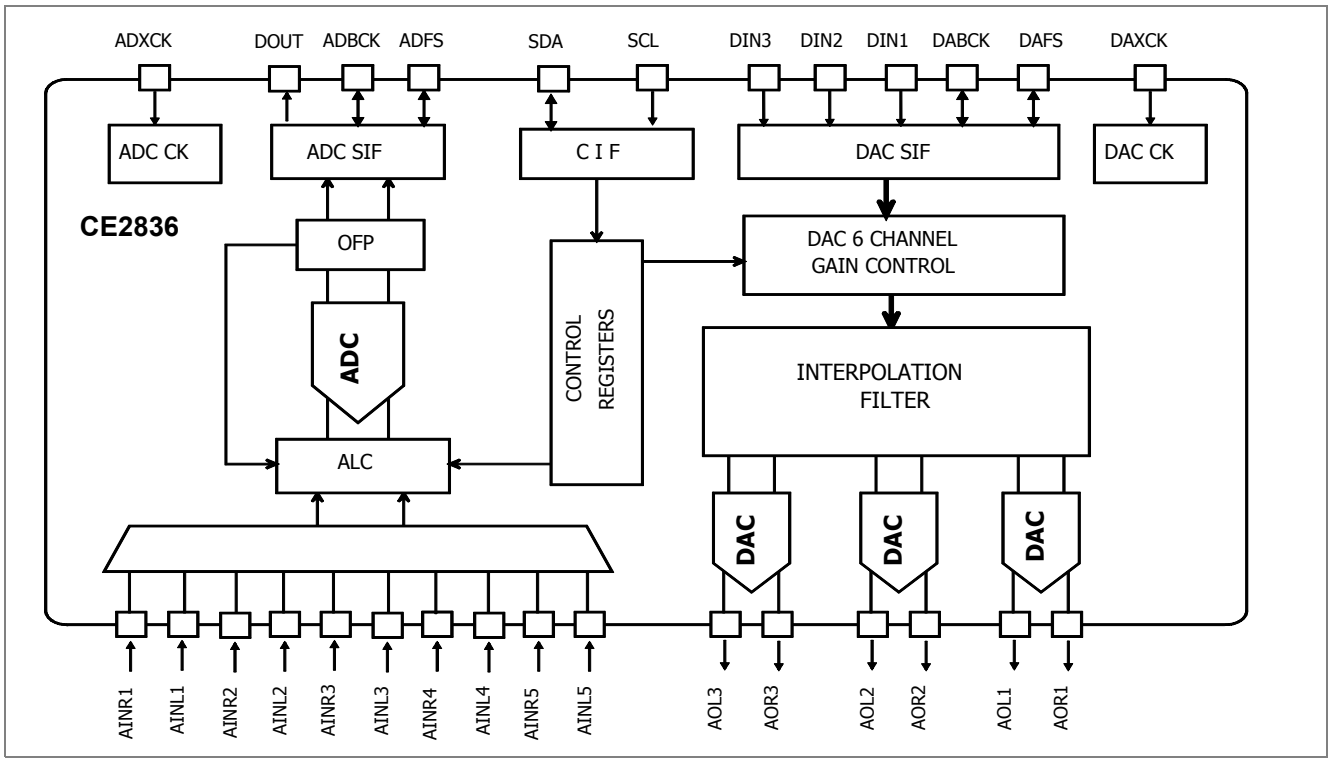
The ADC utilizes cascaded ΣΔ architecture. The internal digital filter has a 20K bandwidth. It support sampling frequency up to 96K Hz. The ADC also includes a analog Automatic Level Control and Noise Gate function to ease the recording applications.

FEATURES

- Six Channel Audio DAC.
  - 104 dB SNR (A Weighted).
  - -82 dB THD + N Ratio (A Weighted).
  - 32K - 192 KHz. Sampling Rates.
  - On -chip Reconstruction Filters.
  - Independent Digital Volume Control.
- Stereo Audio ADC.
  - 5 Channel ADC inputs.
  - Up to 96K Sampling Rate.
  - With Automatic Level Control and Noise Gate.
  - Includes ALC and Noise Gate Functions.
- I^2S, Left and Right Justified Digital I/F Formats.
- 2-wire Serial Control Interface.
- 3.3 Volt Power Supply.

Applications

- Digital Surround Sound For Home Theatre
- DVD or DVD Recordable.



CE2836 Performance

Item	DAC PERFORMANCE SPECIFICATIONS	Spec.
1	Audio Output Level	1 Vrms
2	Audio Bandwidth 20Hz - 20 KHz	+/- 0.1 dB
3	SNR (A-weight)	>104 dB
4	THD + NOISE (A-weight, 0 dB input)	< -82 dB
5	Dynamic Range	94 dB
6	Channel Separation	< -92 dB
7	Nonlinear Distortion	< 0.25 dB
8	Channel Gain Error	< 0.1 dB
	ADC PERFORMANCE SPECIFICATIONS	
1	Maximum Input Level	4 Vpp
2	0 dB Audio Input Level	1 Vrms
3	Audio Bandwidth 20Hz - 20 KHz	+/- 0.5 dB
4	SNR (A-weight)	>98 dB
5	THD + NOISE (A-weight, 0 dB input)	< -88 dB
6	Dynamic Range	94 dB
7	Channel Separation	< -96 dB
8	Nonlinear Distortion	< 0.25 dB
9	Channel Gain Error	< 0.5 dB

All Measurement were taken with only one channel active.

Description (continue)

The DAC support conversion rate from 32K to 192KHz while the ADC from 32K to 96K. The CE2836 support 32, 24, 20 and 16-bit input data. It also support multiple sampling frequency data. Each DAC has its own individual volume control.

XCK REQUIREMENT

The CE2836 supports 32K, 44.1K, 48K, 96K and 192K sampled audio in DAC operations and32K, 44.1K, 48K and 96K sampled audio in ADC operations. The oversampled clock, XCK, requirements are listed in Table 1 and 2.

The DAC and ADC PCM serial port can be configured as '*Master*' or '*Slave*' independently and each has separated over sampling clock input. In the '*Slave Mode*' PCM serial port operation if the AUTODEC, CR1[7]==1,there is an clock frequency detection circuit to set up the system clock, the users don't need to set the SRC registers. However in the '*master mode*' operation the users need to set the SCR registers for the serial audio clock generations

Table 1.

Sampling Rate	DAC XCK Requirement				
		DACDIV==0		DACDIV==1	
32 K	**XCK Freq**	12.288 MHz	8.192 Mhz.	24.576 Mhz	16.384 Mhz
	SRC[1:0]	[11], 384 fs	(#), 256 fs	[11], 768fs	(#), 512 fs
44.1K	**XCK Freq**	16.934 Mhz	11.29 Mhz.	33.869 Mhz	22.579 Mhz
	SRC[1:0]	[11], 384fs	[10], 256 fs	[11], 768 fs	[10], 512fs
48 K	**XCK Freq**	18.432 MHz	12.288 Mhz	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[11], 384 fs	[10], 256 fs	[11], 768fs	[10], 512 fs
96 K	**XCK Freq**	18.432 MHz	12.288 Mhz.	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[01], 192 fs	[00], 128 fs	[01], 384 fs	[00], 256 fs
192 K	**XCK Freq**	18.432 Mhz	12.288 Mhz.	36.864 MHz	24.576 Mhz.
	SRC	(#), 96 fs	(#), 64 fs	(#), 192 fs	(#), 128 fs

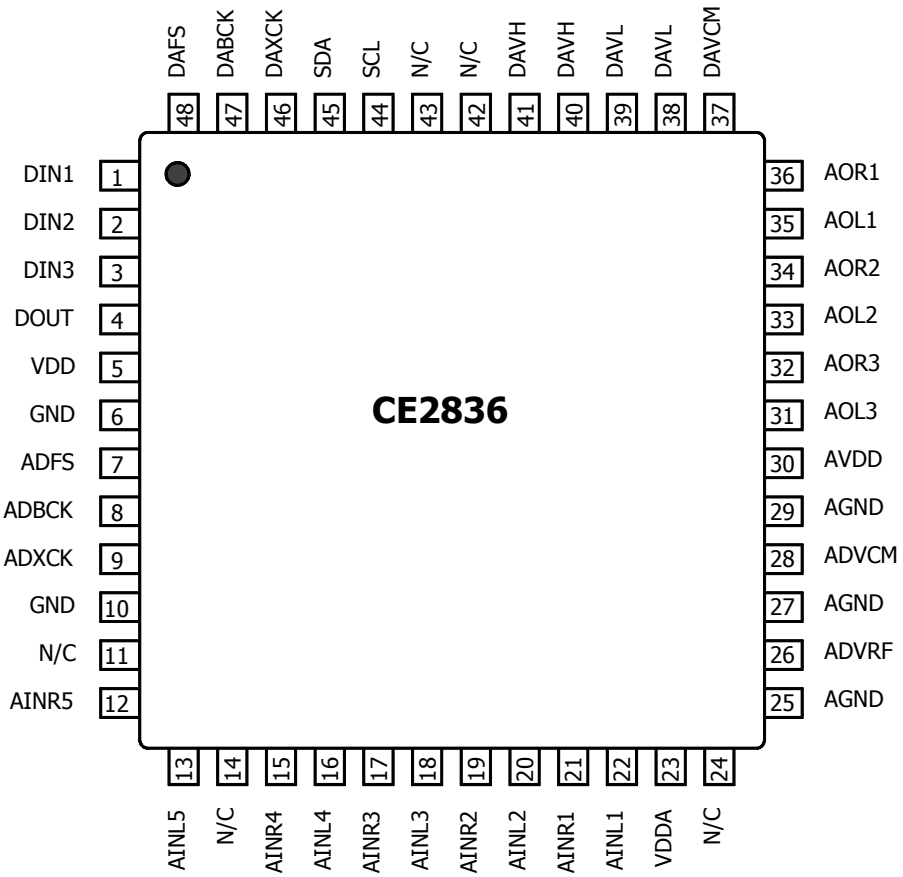
All the XCK clock rate listed are supported in the 'Slave Mode'
SRC Registers are used in the '*Master Mode*'. (#) are not supported in the in the 'Master Mode' .
DAC AUTODET is CREG1[7], DAC SRC[1:0]are CREG1[6:5] and DACDIV is CREG1[4].

Table 2.

Sampling Rate	ADC XCK Requirement				
		DACDIV==0		DACDIV==1	
32 K	**XCK Freq**	12.288 MHz	8.192 Mhz.	24.576 Mhz	16.384 Mhz
	SRC[1:0]	[10], 384 fs	(#), 256 fs	[10], 768fs	(#), 512 fs
44.1K	**XCK Freq**	16.934 Mhz	11.29 Mhz.	33.869 Mhz	22.579 Mhz
	SRC[1:0]	[10], 384fs	[00], 256 fs	[10], 768 fs	[00], 512fs
48 K	**XCK Freq**	18.432 MHz	12.288 Mhz	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[10], 384 fs	[00], 256 fs	[10], 768fs	[00], 512 fs
96 K	**XCK Freq**	18.432 MHz	12.288 Mhz.	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[11], 192 fs	[01], 128 fs	[11], 384 fs	[01], 256 fs

All the XCK clock rate listed are supported in the 'Slave Mode' .
SRC Registers are used in the '*Master Mode*'. (#) are not supported in the 'Master Mode' .
ADC AUTODETis CREG9[7], DAC SRC[1:0]are CREG9[6:5] and DACDIV is CREG9[4].

PIN ASSIGNMENT



PIN DESCRIPTION

Pin Name	Pin #	Type	Description
DIGITAL			
N/C	43		No connection. It can be tied to GND.
SDA	44	I/O	Serial command port data line.
SCL	45	I	Serial command port clock line.
DAXCK	46	I	External master clock input for DAC.
DABCK	47	I	DAC audio serial data clock Input pin (default) if DAC I/F is configured to be ‘slave’ else it is an Output.
DAFS	48	I	DAC left/right channel clock pin. Please refer to Figure 1 PCM data format for its definition Input (default) if DAC I/F is configured to be ‘slave’ else it is an output
DIN1	1	I	DAC Channel 1 or TDM serial audio data input.
DIN2	2	I	DAC Channel 2 serial audio data input.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
DIN3	3	I	DAC Channel 3 serial audio data input.
DOUT	4	O	Serial ADC output
VDD	5	+3.3V	Digital power supply, 3.3 Volt.
GND	6	GND	Digital ground
ADFS	7	I/O	ADC left/right channel clock pin. Please refer to Figure 1 PCM data format for its definition. Input (default) if ADC I/F is configured to be *'slave'* else it is an output
ADBCK	8	I/O	External master clock input for ADC. Input (default) if ADC I/F is configured to be *'slave'* else it is an output
ADXCK	9	I	ADC audio serial data clock input.
GND	10	I	Digital ground
Analog			
N/C	11		No connection. It can be tied to AGND.
AINR5	12	I	ADC channel 5 right input. Input resistance is 20K Ohm
AINL5	13	I	ADC channel 5 left input. Input resistance is 20K Ohm
N/C	14		No connection. It can be tied to AGND.
AINR4	15	I	ADC channel 4 right input. Input resistance is 20K Ohm
AINL4	16	I	ADC channel 4 left input. Input resistance is 20K Ohm
AINR3	17	I	ADC channel 3 right input. Input resistance is 20K Ohm
AINL3	18	I	ADC channel 3 left input. Input resistance is 20K Ohm
AINR2	19	I	ADC channel 2 right input. Input resistance is 20K Ohm
AINL2	20	I	ADC channel 2 left input. Input resistance is 20K Ohm
AINR1	21	I	ADC channel 1 right input. Input resistance is 20K Ohm
AINL1	22	I	ADC channel 1 left input. Input resistance is 20K Ohm
AVDD	23	+3.3V	ADC power supply.
N/C	24		No connection. It can be tied to AGND.
AGND	25	GND	Analog ground pin.
ADVRF	26	O	ADC reference voltage. It should be decoupled to AGND with a 22 uF capacitor in parallel with a 0.1 uF. Its value should be AVDD/2 volt.
AGND	27	GND	Analog ground pin.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
ADVCM	28	O	ADC comment mode voltage. It should be decoupled to AGND with a 22 uF in parallel with a 0.1 uF. Signal level is AVDD/2.
AGND	29	GND	Analog ground pin.
AVDD	30	+3.3V	DAC power supply.
AOL3	31	O	Analog left channel 3 output
AOR3	32	O	Analog right channel 3 output
AOL2	33	O	Analog left channel 2 output
AOR3	34	O	Analog right channel 2 output
AOL1	35	O	Analog left channel 1 output
AOR1	36	O	Analog right channel 1 output
DAVCM	37	O	DAC comment mode voltage. It should be connected to a 22 uF in parallel with a 0.1 uF decoupling capacitors to ground. Signal level is AVDD/2.
DAVL	38, 39	GND	DAC negative reference voltage. It should be tied to AGND.
DAVH	40,41	I	DAC positive reference voltage. It should be connected to AVDD via a 180 ohm serial resistor, and a 22 uF in parallel with a 0.1 uF decoupling capacitors to ground.
N/C	42		No connection. It can be tied to AGND.

DIGITAL AUDIO SERIAL INTERFACE

There are two independent PCM serial ports, one for DAC and one for ADC. The DAC digital serial interface consists of 3 serial input pins, DIN1, DIN2, DIN3, one serial clock input/output pin, DABCK, and one left/right indicator input/output pin, DAFS. The ADC consists of a data output pin, DOUT and one serial clock input/output pin, ADBCK, and one left/right indicator input/output pin, ADFS. The BCK and FS are output pins when the respective port is configured as '*Master*', and input pin when it is configured as '*Slave*' port. The Master/Slave operations are setup via CREGA[7] and CREGA[3]. The data are 2's complement MSB first numbers. The CE2836 supports four resolution, which are selected programming the control register CREG0 and CRFEGA via the I^2C serial control port. Table 3 describes these four resolution.

Table (3): Audio Serial Data Input Resolution,

Format	NBIT[1:0]	DIN, DOUT
0	00	16-bit
1	01	20-bit
2	10	24-bit (default)
3	11	32-bit

The DIN and DOUT can be either 24-bit or 32-bit per frame as well as left justified, right justified or I2S. .

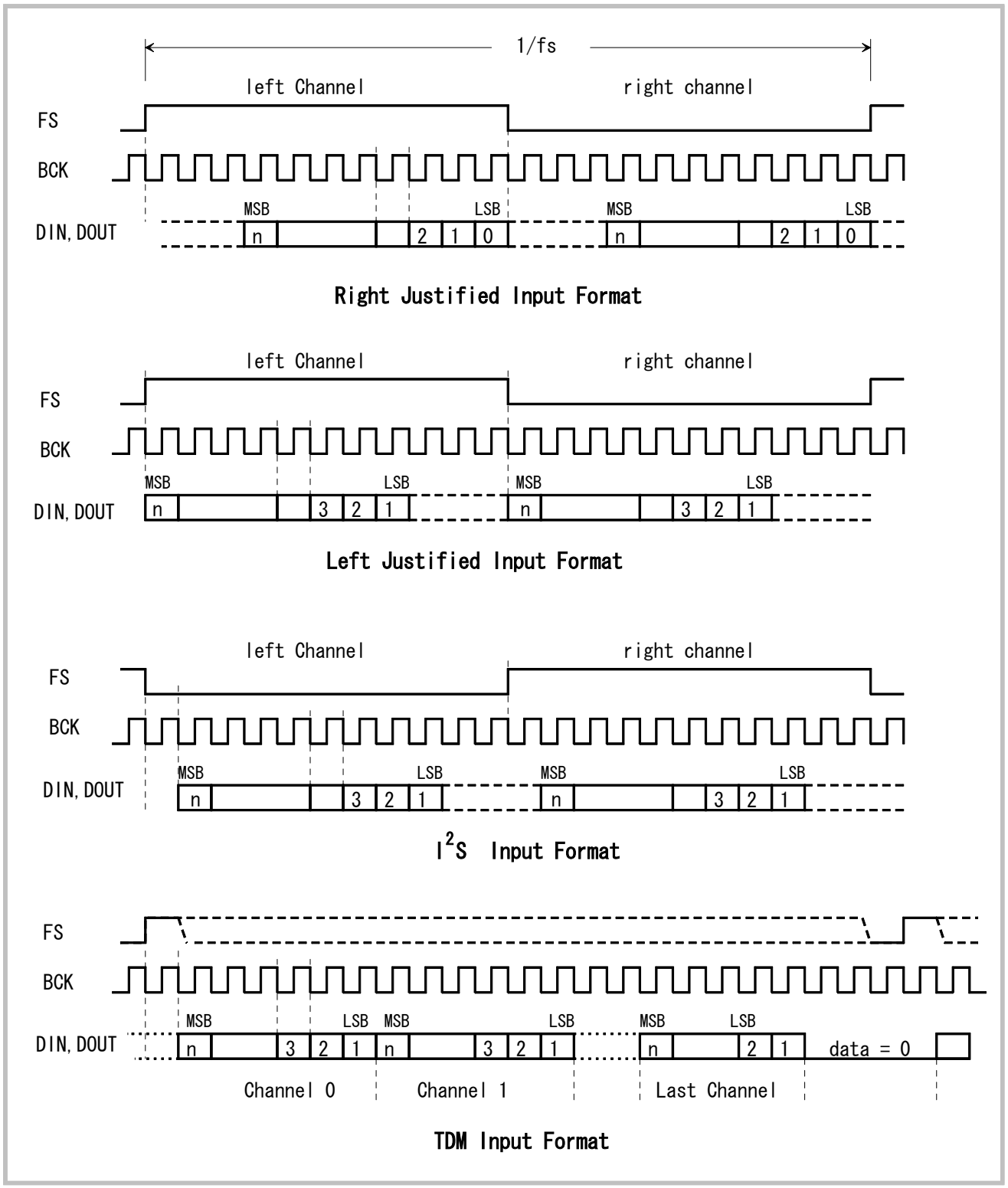
Table (4): Audio Serial Data Input Modes

Mode	FMT[1:0]	DIN, DOUT
0	00	Right Justified
1	01	Left Justified
2	10	I2S (default)
3	11	TDM

TDM Input Format

The CE2836 support Time Division Multiplex data input. In this format only one data input pin is required. The six channel data are sent in serial order, channel 1 first, followed by channel 2 and so forth. The number of bits per channel is defined by CREG0[5:4].

Figure 1. Audio Serial Input Data Format



DAC INFINITE ZERO DETECTION

The CE2836 DAC has an Infinite Zero Detection circuit which detects zero in the Audio Serial Port that lasts for approximately 0.2 sec. By default, the zero detection circuit is on.

DAC Digital Attenuation

Each DAC contains an Digital Attenuation block. The attenuation values are hold in the Volume Control Registers. The Value 80H corresponds to Full Scale, 0dB. and each decrement correspond to -0.5 dB additional attenuation.

ADC Gain and ALC

Each channel of ADC input includes a Analog Gain. The Gain is controlled by CREGC, ADC Gain Selection, The gain range is from +6 dB to -9 dB. with 1 dB step. The GAIN = 9 corresponds to 0dB gain. The AUTOMATIC LEVEL CONTROL set the ADC maximum digital output to a prescribed value by automatic manipulating the analog gain. The ALC is controlled by CREG8, ADC PROC. REGISTER..

Table (5): ALC Target Level

ALC[2:0]	Maximum Digital Output
000	-1 dB FS
001	-2 dB FS
010	-3 dB FS
011	-4 dB FS
100	-5 dB FS
101	-6 dB FS
110	-7 dB FS
111	-8 dB FS

Table (6): ALC Hold Time

ALCHTM	Hold Time	Comment
0	340 msec.	For music program
1	5.3 msec	For speech program

ADC Noise Gate

Noise Gate remove hissing noise during silence period. It is useful for recording noisy program. While Noise Gate is enabled the ADC digital output will be zeroed if the signal level below a predetermined value for about 0.5 seconds. The noise Gate is controlled by the same ADC PROC. REGISTER.

Table (7): Noise Gate Threshold

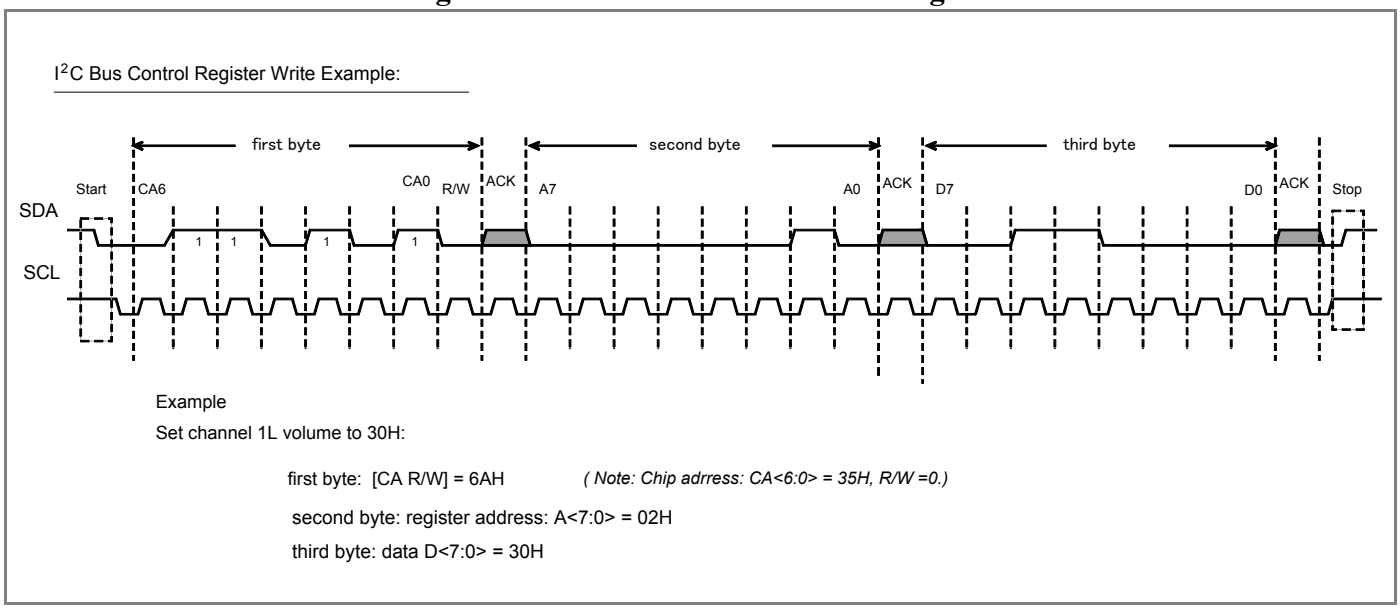
NGTH[1:0]	Threshold
00	-66 dB
01	-72 dB
10	-78 dB
11	-84 dB

Serial Command Port

The user can select the chip operation mode by programming the internal control registers through serial I^2C port. The Chip Address for the CE2836 is 35H. The protocol for write operation consists of sending 3 byte data to CE2836, following each byte is the acknowledges generated by CE2836. The first byte is the 7-bit Chip Address followed by the read/write bit (read is high, write is low). The second byte is the control register address. The third byte is the control register data.

Upon power up, all programmable registers are set to default values. Figure 2 describes the serial command port timing relationship.

Figure 2. Serial Command Port Timing



SERIAL PORT CONTROL REGISTER ASSIGNMENT

There are 8 registers dedicated to the CE2836 for chip functional programming, The register addresses assignments are

Address (decimal)	Register	Default Value	Register Function
0	CREG0[7:0]	A0	DAC Control REG0: Data input format, de-emphasis filter selection
1	CREG1[7:0]	80	DAC Control REG1: Input format and PLL output frequency selection
2	CREG2[7:0]	80	Volume Control Register for DAC channel 1, left
3	CREG3[7:0]	80	Volume Control Register for DAC channel 1, right
4	CREG4[7:0]	80	Volume Control Registerl for DAC channel 2, left
5	CREG5[7:0]	80	Volume Control Register for DAC channel 2, right
6	CREG6[7:0]	80	Volume Control Register for DAC channel 3, left
7	CREG7[7:0]	80	Volume Control Registerl for DAC channel 3, right
8	CREG8[7:0]	82	ADC Proc REG: ALC and Noise Gate Control Registers
9	CREG9[7:0]	A0	ADC Control Register.
10	CREGA[7:0]	00	CHIP Control Register.
11	CREGB[7:0]	01	ADC MUX Select.
12	CREGC[7:0]	99	ADC Input Gain Select
13	CREGD[7:0]	92	Chip Soft Reset.

CONTROL REGISTERS DESCRIPTION

CREG0, DAC Control Register 0 (ADRS=hex00, default=hexA0)

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 00	FMT[1:0]		NBIT[1:0]		AMUTE	DEEMP	FSMPL[1:0]	
Default Value	1	0	1	0	0	0	0	0

FMT[1:0] Digital Serial Bus Format Select
- 00: - Normal or Right Justified Format.
- 01: -Left Justified Format.
- 10: - I2S Format.(default)
- 11: - TDM, Multi-channel Time Division Multiplex Format

NBIT[1:0]: - These two bits define the serial audio input resolution for right justified and TDM mode
- 00: - 16-bit resolution.
- 01: - 20-bit resolution.
- 10: - 24-bit resolution (default).
- 11: - 32-bit resolution.

AMUTE: - Auto-mute detection enable.
- 0: - Auto-mute enabled. (default)
- 1: - No auto-mute.

DEEMP: - Enable de-emphasis
- 0: - Normal. (default)
- 1: - enable de-emphasis.

FSMPL: - Interpolation filter selection.
These two bits are recognized only when “AUTODET” bit of the CREG1 is set to ‘0’.
- 0X: - 44.1 or 48K sampling.(default)
- 10: - 96K sampling.
- 11: - 192K sampling.

CREG1, DAC Control Register 1(ADRS=hex01, default=hex80)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 01	AUTODET	SRC[1:0]		CKDIV2	X	MUTE56	MUTE34	MUTE12
Default Value	1	0	0	0	0	0	0	0

AUTODET Automatically detects the serial audio input data sampling rate clock frequency.
0: - do not use auto-detect
1: - automatically detects the serial audio input data sampling rate and clock frequency.

SRC[1:0]: - DAC Sampling Rate Selection. It is used in the DAC Master Mode, CRA[7]==1, to generate DAFS and DABCK.

00: - Sampling Rate = XCK/128.
01: - Sampling Rate = XCK/192.
10: - Sampling Rate = XCK/256.
11: - Sampling Rate = XCK/384.

CKDIV2: - Enable the ADXCK Clock divided by 2.
0: - DAC system clock is DAXCK (default)
1: - DAC system clock is DAXCK/2

MUTE56: Mute control for channels 5 and 6
0: do not mute channels 5 and 6
1: simultaneously mute channels 5 and 6

MUTE34: Mute control for channels 3 and 4
0: do not mute channels 3 and 4
1: simultaneously mute channels 3 and 4

MUTE12: Mute control for channels 1 and 2
0: do not mute channels 1 and 2
1: simultaneously mute channels1 and2

CREG2 - 7, DAC Volume Registers for channel 1 to 6, (ADRS=hex02 - hex07, default=hex80)

ADDR[3:0]	Volume Registers							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 02	Channel 1 left volume register, VOLREGL1[7:0]							
Hex 03	Channel 1 right volume register, VOLREGR1[7:0]							
Hex 04	Channel 2 left volume register, VOLREGL2[7:0]							
Hex 05	Channel 2 right volume register, VOLREGR2[7:0]							
Hex 06	Channel 3 left volume register, VOLREGL3[7:0]							
Hex 07	Channel 3 right volume register, VOLREGR3[7:0]							
Default Value	1	0	0	0	0	0	0	0

VOLREG:- Control the volume of the 6 DAC's

80h corresponds to 0 dB and 02h to -64 dB. in -0.5 db step. Value should not be programmed greater than 80h.

CREG 8, ADC Proc Register (ADRS=hex08, default=hex82)

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 08	NGATE	NGTH[1:0]		ALCHTM	ALCEN	ALC[2:0]		
Default Value	1	0	0	0	0	0	1	0

NGATE: Noise Gate
- 0: - Noise Gate Disabled.
- 1: -Noise Gate Enable. When the signal level is lower than the level specified by the NGTH the ADC output will be zeroed.

NGTH[1:0]: - Specified the Noise Gate Threshold.
- 00: - -66dB
- 01: - -72 dB.
- 10: - -78dB.
- 11: - -84 dB.

ALCHTM: - Automatic Level Control Hold time.
- 0: - 340 ms. (default). For music program.
- 1: - 5.3 ms. This should be used for speech conversion.

ALCEN: - Enable Automatic Level Control Function
- 0: - Disable ALC. (default)
- 1: - Enable ALC.

ALC[2:0]: - ALC Target Level.
- 000: - -1 dB.
- 001: - -2 dB.
- 010: - -3 dB. (default)
- 011: - -4 dB.
- 100: - -5 dB.
- 101: - -6 dB.
- 110: - -7 dB.
- 111: - -8 dB.

CREG9, ADC Control Register (ADRS=hex09, default=hexA0)

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 09	FMT[1:0]		NBIT[1:0]		X	SRC[1:0]		CKDIV2
Default Value	1	0	1	0	0	0	0	0

MT[1:0] Digital Serial Bus Format Select for ADC.
- 00: - Normal or Right Justified Format.
- 01: -Left Justified Format.
- 10: - I2S Format.(default)
- 11: - TDM, Multi-channel Time Division Multiplex Format

NBIT[1:0]: - These two bits define the ADC serial audio input resolution for right justified and TDM mode
- 00: - 16-bit resolution.
- 01: - 20-bit resolution.
- 10: - 24-bit resolution (default).
- 11: - 32-bit resolution.

SRC[1:0]: - ADC Sampling Rate Selection. It is used in the ADC Master Mode, CRA[1]==1, to generate ADFS and ADBCK.

- 00: - Sampling Rate = XCK/256.
- 01: - Sampling Rate = XCK/128.
- 10: - Sampling Rate = XCK/384.
- 11: - Sampling Rate = XCK/192.

CKDIV2: - Enable the ADXCK Clock divided by 2.
- 0: - ADC system clock is ADXCK (default)
- 1: - ADC system clock is ADXCK/2

CREGA, Chip Control Register (ADRS=hex0A, default=hex00)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0A	DAMSTR	DAPWD	X	X	ADMSTR	ADPWD	ZCBYP	HPFBYP
Default Value	0	0	0	0	0	0	0	0

DAMSTR: Configure the DAC PCM Serial Port.
- 0: - Slave Mode
- 1: - Master Mode.

DAPWD: DAC Power Down
- 0: DAC enabled
- 1: DAC Power Down.

ADMSTR: Configure the ADC PCM Serial Port.
- 0: - Slave Mode
- 1: - Master Mode.

ADPWD: ADC Power Down
- 0: ADC enabled
- 1: ADC Power Down.

ZCBYP: Disable ADC Zero Crossing Detection
- 0: Zero crossing is enabled.
- 1: Zero crossing is bypassed.

HPFBYP: Bypass ADC data path High Pass Filter
- 0: Enable high pass filter.
- 1: Disable high pass filter.

CREGB, ADC Input Enable (ADRS=hex0B, default=hex01)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0B	X	X	X	AMUX[4:0]				
Default Value	1	0	0	0	0	0	0	1

AMUX[4:0]: ADC Input Channel Enable.
00001: - AIN1
00010: - AIN2
00100: - AIN3
01000: - AIN4
10000: - AIN5

CREGC, ADC Input Gain Selection (ADRS=hex0C, default=hex99)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0C	LGAIN[3:0]				RGAIN[3:0]			
Default Value	1	0	0	1	1	0	0	1

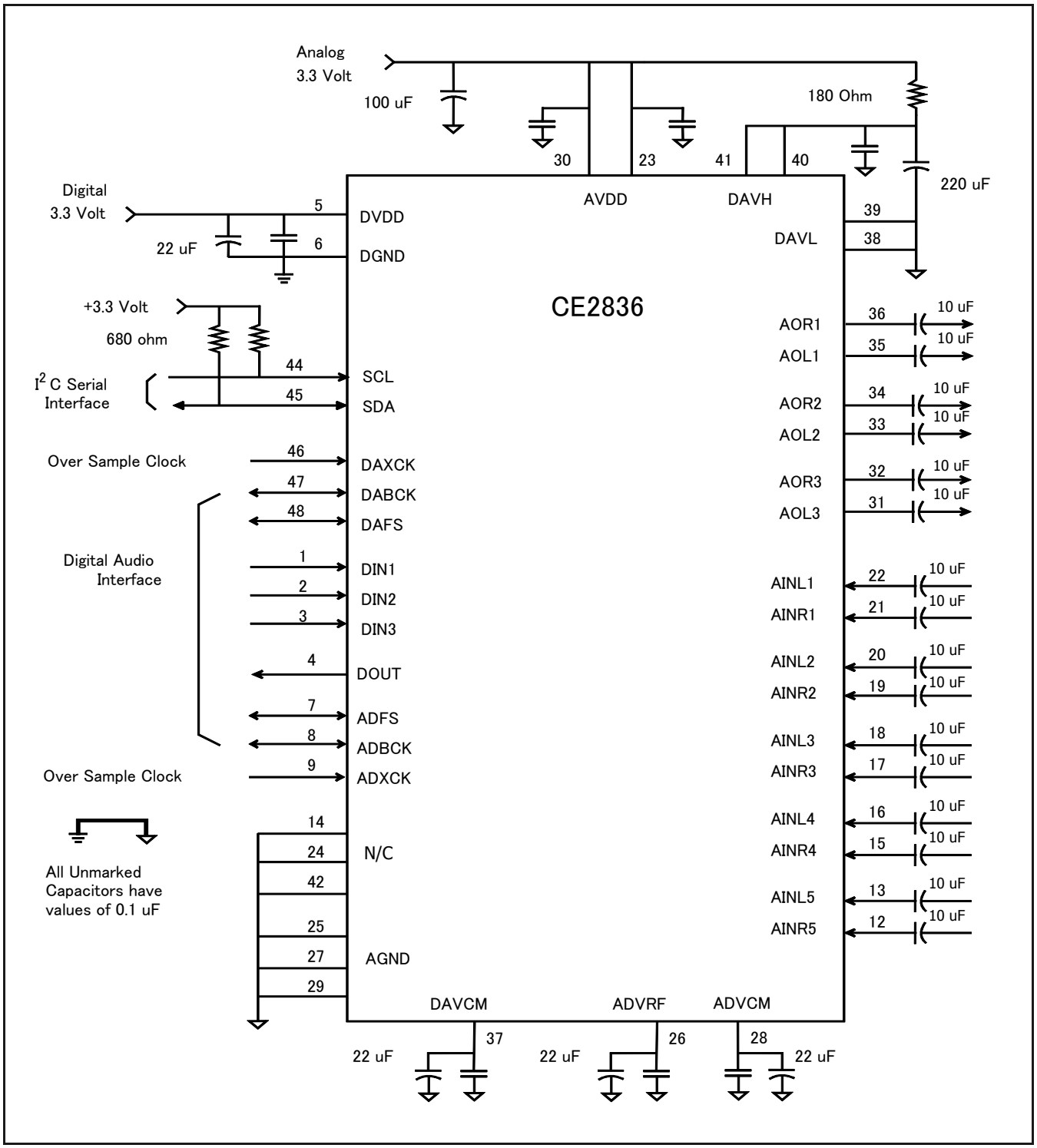
LGAIN[3:0] is for ADC Left Channel Gain Select While RGAIN[3:0] is for Right Channel Gain Select
1111 corresponds to +6 dB and 0000 to -9 dB with -1dB step

CREGD, Chip Soft Reset (ADRS=hex0D, default=hex92)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0D	RESET[7:0]							
Default Value	1	0	0	1	0	0	1	0

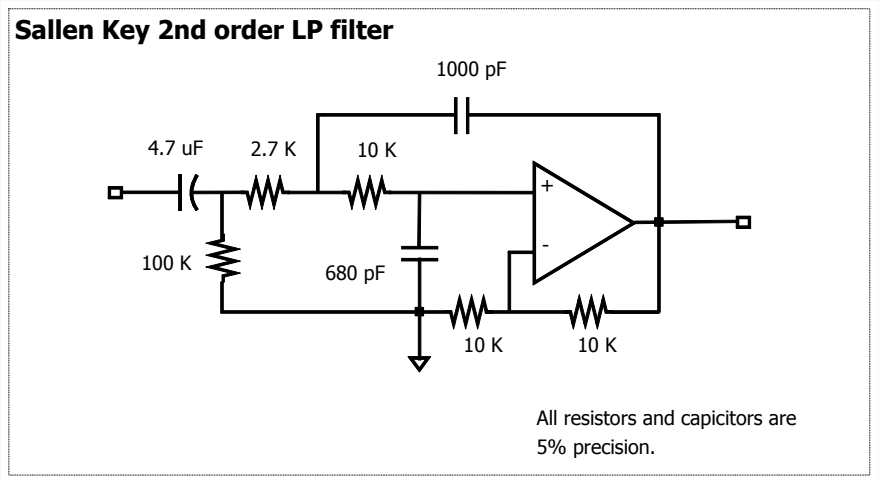
Chip Soft Reset; A write of all zeros to this register will reset the chip except the Command Registers. Another write of hex92 is required to enable to chip again.

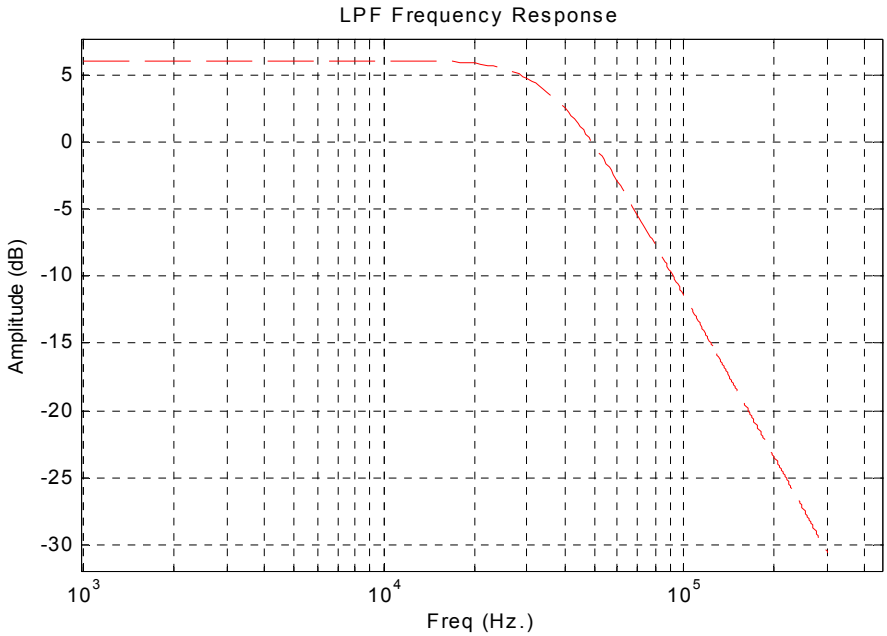
APPLICATION CONNECTION EXAMPLE:



SUGGESTED ANALOG RECONSTRUCTION FILTER

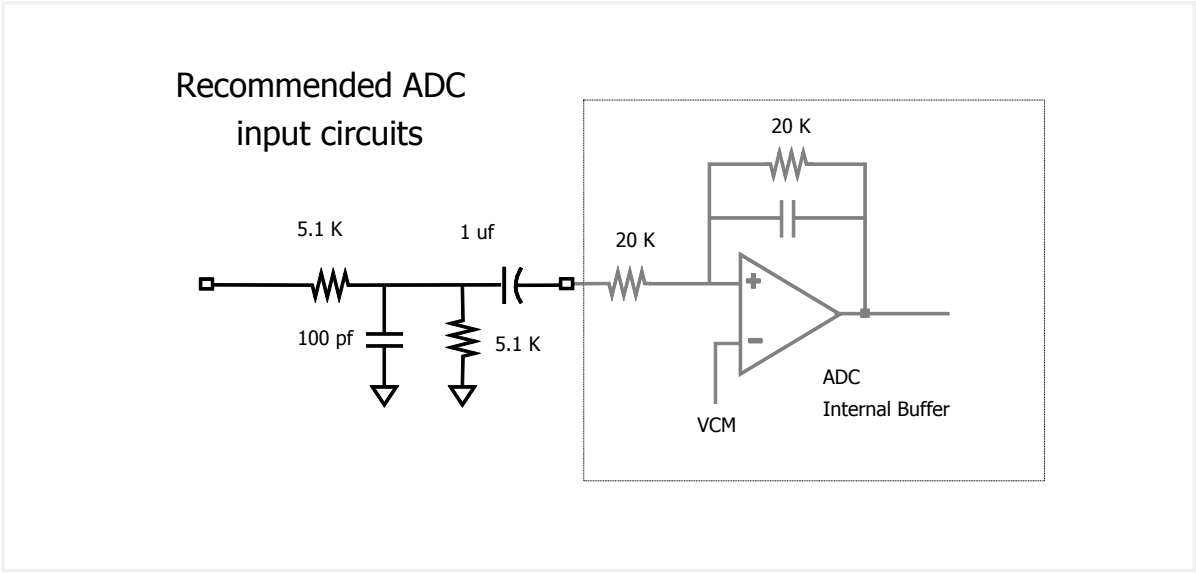
A second Sallen Key low pass reconstruction filter is recommend to remove the high frequency sigma delta modulator noise. The filter's component values and characteristic are shown in the following figures.





ADC

The ADC converters have a input buffer. The buffers have a equivalent input resistance of 20K ohm. To ensure the performance it is recommended that the applications should have a simple low pass filter to remove the high frequency noise.



TIMING DIAGRAM

Figure 3. Audio Serial Interface Timing Requirement

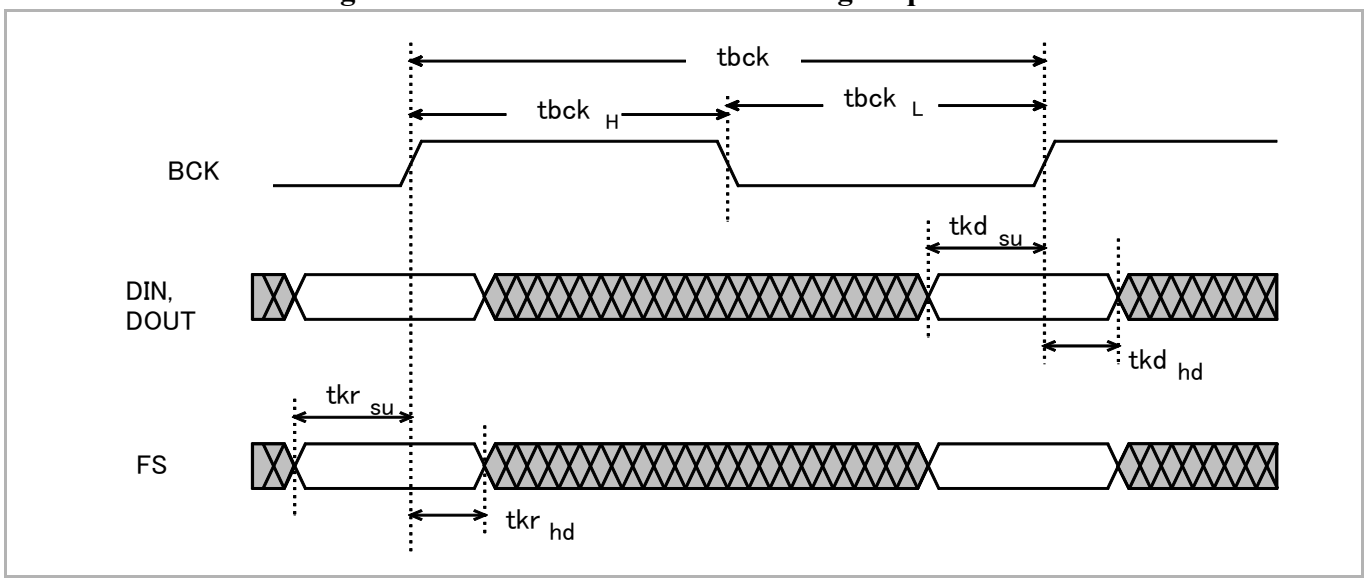
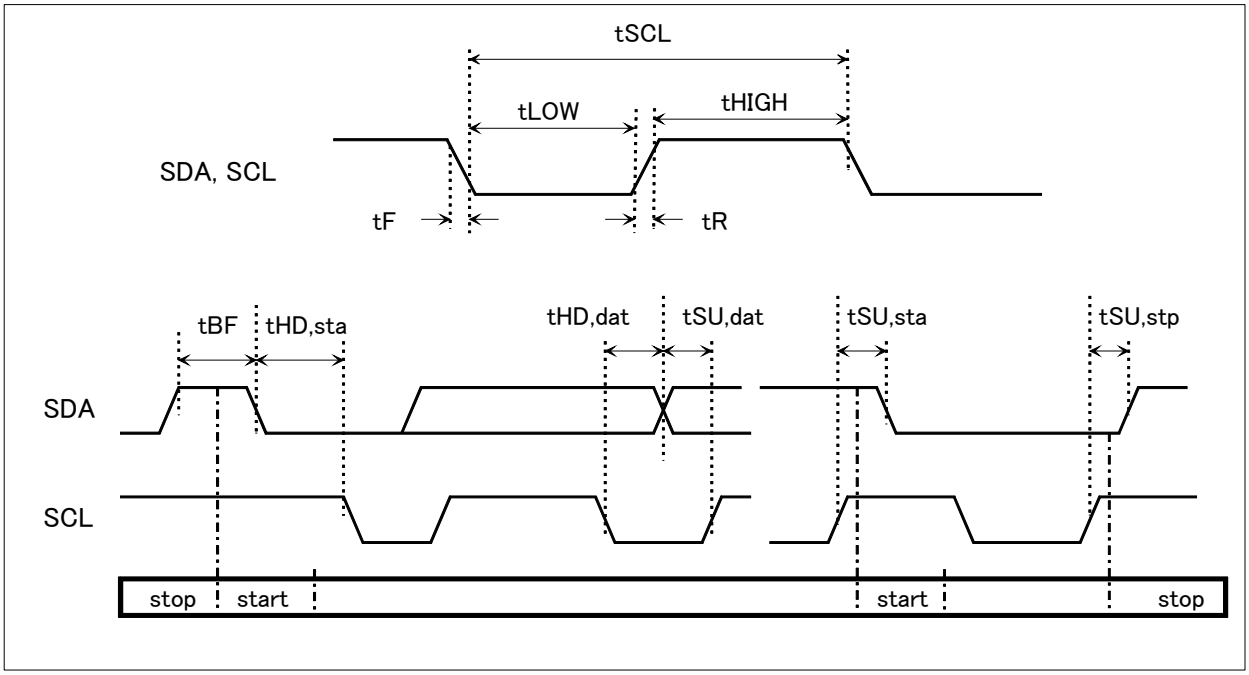


Figure 4. Serial Command Port Write Timing Requirement



ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Units
V_{DD}	Power Supply Voltage (Measured to GND)	-0.5	+7.0	V
V_i	Digital Input Applied Voltage[2]	GND-0.5		V
A_i	Digital Input Forced Current[3,4]	-100	100	mA
V_o	Digital Output Applied Voltage[2]	GND-0.5	V_{DD}+0.5	V
A_o	Digital Output Forced Current[3,4]	-100	100	mA
TDsc	Digital Short Circuit Duration (single output high state to Vss)		1	Sec
TA_{SC}	Analog Short Circuit Duration (single output to VSS1)		infinite	Sec
T_a	Ambient Operating Temperature Range	-25	+125	°C
T_j	Junction Temperature (Plastic Package)	-65	+150	°C
Tsol	Lead Soldering Temperature (10 sec., 1/4" from pin)		280	°C
Tvsol	Vapor Phase Soldering (1 minute)		220	°C
Tstor	Storage Temperature	-65	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.

2. Applied voltage must be current limited to specified range, and measured with respect to VSS.

3. Forcing voltage must be limited to specified range.

4. Current is specified as conventional current, flowing into the device.

ELECTRICAL CHARACTERISTICS

Parameter	Characteristics	Min	Typ	Max	Units
Power Supply					
AVDD	Analog power supply voltage	2.8	3.3	4.0	V
DVDD	Digital power supply voltage	2.8	3.3	4.0	V
I_{DA}	Analog Current		60		mA
I_{DD}	Digital Current		20	18	mA

Audio DAC Characteristics

	Full Scale Output Voltage to a 10K load	.98	1	1.02	Vrms
V_{VCM}	Reference voltage		VDD/2		V

Digital Characteristics

V_{IH}	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V_{DD}	V
I_{OZH}	Hi-Z Leakage Current, HIGH, V_{DD}=Max, V_{IN}=3.3 Volt			33	μ A
I_{OZL}	Hi-Z Leakage Current, LOW, V_{DD}=Max, V_{IN}=$V_{SS)}$			-10	μ A
C_I	Digital Input Capacitance (T^A=25°C, f=1Mhz)			8	pF
C_O	Digital Output Capacitance (T^A=25°C, f=1Mhz)			10	pF

Audio Serial Interface Timing

tbck	BCK Cycle Time	80			ns
$tbck_H$	BCK Pulse Width, HIGH	30			ns
$tbck_L$	BCK Pulse Width, LOW	30			ns
tkd_{su}	Audio Data Setup Time With Respect To Rising Edge of BCK	10			ns
tkd_{hd}	Audio Data Hold Time With Respect to Rising Edge of BCK	15			ns
tkr_{su}	Audio FS Setup Time With Respect To Rising Edge of BCK	10			ns

Parameter	Characteristics	Min	Typ	Max	Units
tkr_{hd}	Audio FS Hold Time With Respect To Rising Edge of BCK	15			ns

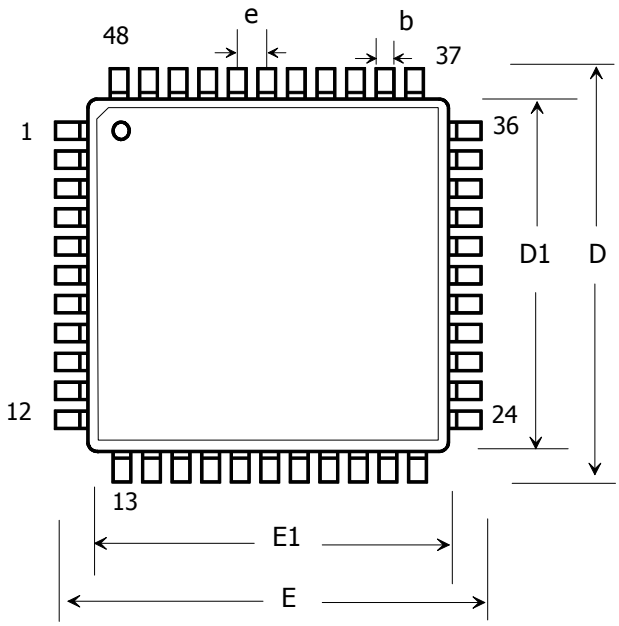
Serial Command Port

fSCL	SCL Clock Frequency			100	kHz
tSU,sta	Start condition set up time	4.7			us
tHD,sta	Start condition hold time	4.0			us
tSU,stp	Stop condition set up time	4.0			us
tLOW	SCL Low time	4.7			us
tHIGH	SCL High time	4.0			us
tR	SCL & SDA rise time			1.0	us
tF	SCL & SDA fall time			0.3	us
tSU,DAT	Data set-up time	250			ns
tHD,DAT	Data hold time	0			ns
tBF	Bus Free time	4.7			us

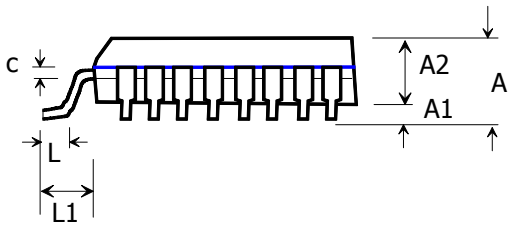
PACKAGING INFORMATION (LQFP 48 PIN)

Dimensions

SYMBOLS	mm.			SYMBOLS	mm.		
	min	norm	max		min	norm	max
A			1.68	E	9.0 BSC		
A1	0.05		0.15	E1	7.0 BSC		
A2	1.35	1.4	1.45	e	0.45	0.65	0.75
b	0.17	0.22	0.27	L	0.63	0.6	1.03
C	0.09		0.20	L1	1.00 REF		
D	9.0 BSC						
D1	7.0 BSC						



LQFP 48 (7 X 7 mm)



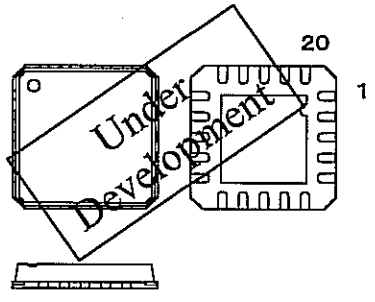
Digital Power Amplifier R2S15102NP

10Wx2ch(SE)/20Wx1ch(BTL) Digital Audio Power Amplifier

1.Outline

R2S15102NP is a Digital Power Amplifier IC developed for TV.
R2S15102NP can realize maximum Power 10W × 2ch
(VD = 24V,THD = 10%, SE) at 8 Ω load.
It is possible to replace from the conventional analog amplifier system to the digital amplifier system easily.

Fig. 1 Package



20pin QFN
Body : 6 x 6 mm
Lead pitch : 0.8 mm

2.Feature

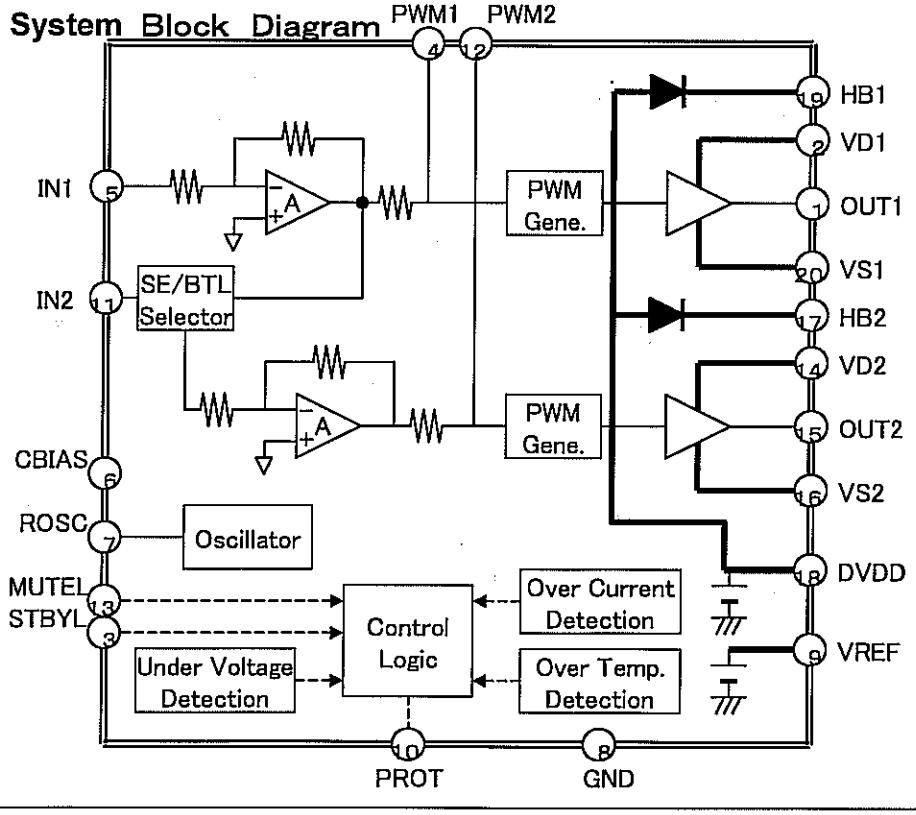
- High Output Power(THD=10%)without external Heat Sink
  (note) the thermal pad is soldered the thermal pad with the printed-circuit board directly.
  Recommanded Power Condition
  SE operation mode :10Wx2ch(VD=24V) at 8 Ω
  BTL operation mode: 20Wx1ch(VD=18V) at 8 Ω
- The RENESAS original circuits realize high power efficiency, low noise and low distortion characteristics.
- Pop sound Less
- Built-in protection function
  (Over Current, Over Temperature and Under Voltage)
- Built-in Mute and Stand-by function

3.Operating Condition

- Recommanded Power supply voltage : from 11V to 25V
- Recommanded Speaker Impedance : from 4 to 8Ω

4.Block Diagram

Fig. 2 System Block Diagram



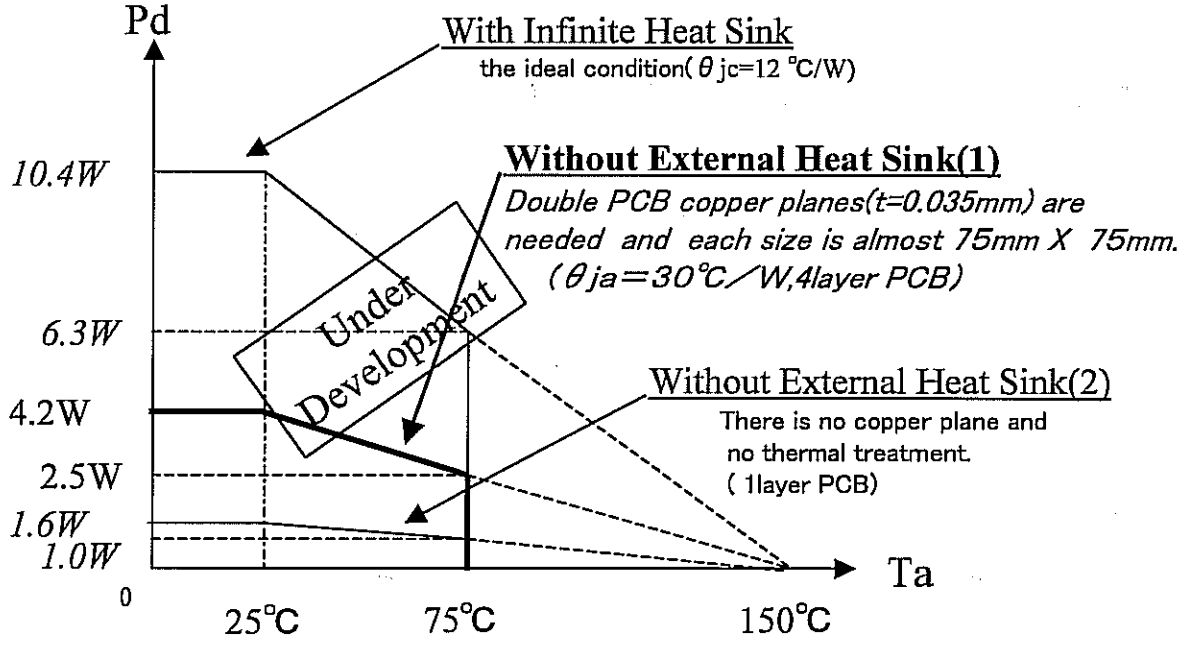
5. Pin Configuration(Table.1)

No.	NAME	I/O	Description	
1	OUT1	O	Power Output pin #1	
2	VD1	—	Power supply pin for power output stage #2	
3	STBYL	I	Stand-by control pin. When this is "L", circuit current is reduced.There is the pull-down resistor:50Kohm(typ.).	
4	PWM1	I	PWM input pin #1 (for phase compensation)	
5	IN1	I	Analog input #1. The gain is depended on the external resistance .	
6	CBIAS	I/O	A capacitor is connected so that it may not be influenced of power supply change(Ripple Filter).	
7	ROSC	I	Control pin for PWM carrier frequency	
8	GND	—	GND pin for analog block	
9	VREF	I/O	Capacitor connection pin for analog block reference voltage source	
10	PROT	O	Protection Timer pin. At protection mode,the output becomes "L"-level. (The timing capacitor is connected)	
11	IN2	I	SE operation	Analog input #2(as same as IN1)
		I	BTL operation	When this is connected to DVDD pin via the resister, Reversed signal of OUT1 is output to OUT2.
12	PWM2	I	PWM input pin#2 (for phase compensation)	
13	MUTEL	I	Mute control pin. When this is "L", it becomes mute status.	
14	VD2	—	Power supply pin for power output stage #2	
15	OUT2	O	Power Output pin #2	
16	VS2	—	Ground pin for power output stage #2	
17	HB2	I/O	Capacitor connection pin for bootstrap	
18	DVDD	O	Built-in power supply pin for internal digital block.	
19	HB1	I/O	Capacitor connection pin for bootstrap #1	
20	VS1	—	Ground pin for power output stage #1	

6. Absolute Maximum Rating(Table.2)

Symbol	Parameter	Condition	Value	Unit
VD max	Maximum VD Voltage	VD1,VD2 pin voltage	27	V
HB max	Maximum HB Voltage	HB1、HB2 pin voltage	40	V
Pd	Power dispassion	Ta = 25°C :See Fig.3	4.2	W
θja	Thermal Resistance	See Fig.3	30	°C/W
Tj	Junction temperature	Maximum Temperature	150	°C
Ta	Operating ambient temperature	Temperature range	-20～75	°C
Tstg	Storage temperature	Temperature range	-40～150	°C

Fig.3 Thermal De-rating(on PCB: printed-circuit board):Size 75mm x 75mm

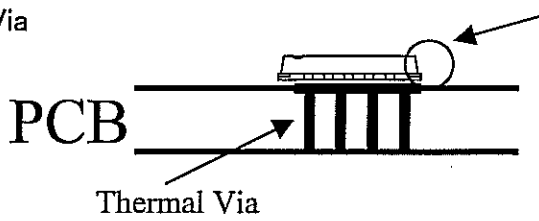


(NOTE)

PCB pattern design for high effective thermal conductivity

(1)The exposed die pad is directly soldered with the printed-circuit board pattern .

(2)Thermal Via



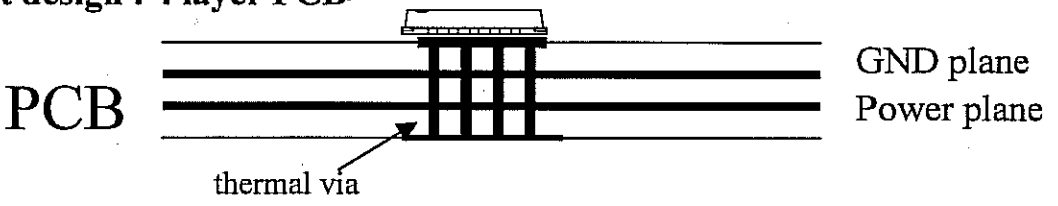
(caution)
There are side expositions of the die pad at corners of the package.
(The die pad is grounded.)

Consideration about the PCB design

The Power dispassion at 10Wx2ch(SE) or 20Wx1ch(BTL) is estimated almost 2W. It has enough margin, designing the PCB at θja=30°C/W.

(1)PCB basic design (copper plane)

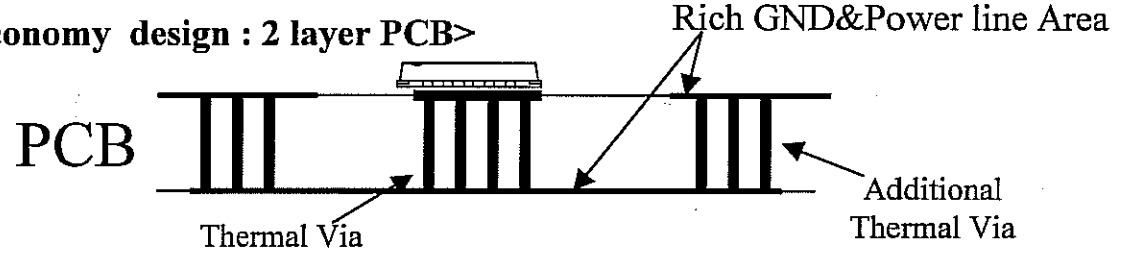
<the best design : 4 layer PCB>



<PCB size estimation >

10Wx2ch: 75mm x 75mm

<the economy design : 2 layer PCB>



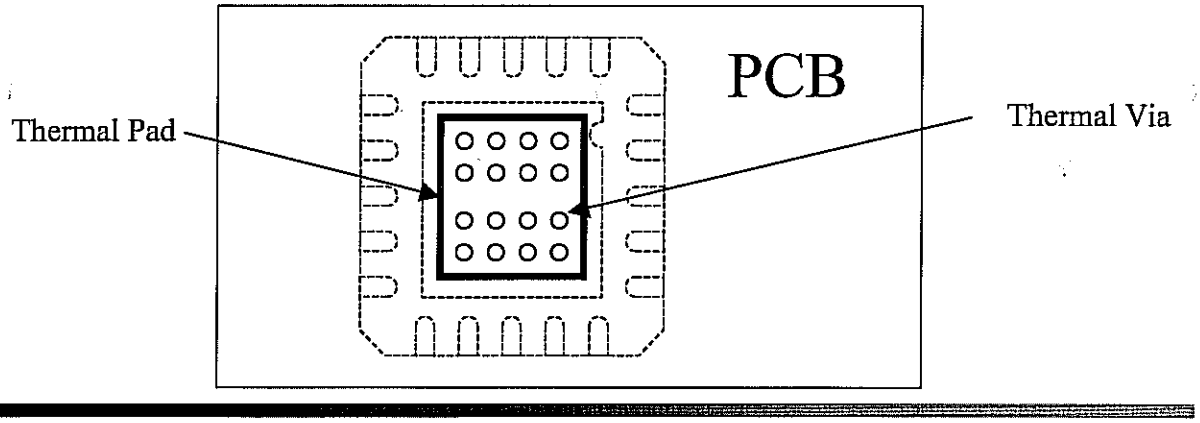
The GND&Power line total area size is also equal to the above GND&Power line total area size of the 4layer PCB.

<PCB size estimation >

10Wx2ch: (75+α)mm x (75+α) mm

(2)PCB Thermal Pad

The exposed die pad is directly soldered with the printed-circuit board pattern .



7. Recommended Operating condition(Table.3)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VD	Supply Voltage	VD1,VD2 pin voltage	11	-	25	V
VH	Control voltage of high level	STBYL、MUTEL	2	-	5	V
VL	Control voltage of low level	STBYL、MUTEL	0	-	0.8	V
fosc	Carrier Frequency	R= 33kΩ	300	400	600	kHz

(note)
- STBYL: High level:normal operation Low level:Stand-by
- MUTEL:High level:normal operation Low level:Mute
- The carrier frequency can be changed by the resistance at Pin#.7 .

8. Electronic Characteristics(Table.4)

(Unless otherwise noted, Ta=25°C, VD=24V, Carrier Frequency=400kHz, f=1kHz,SE operation)

Symbol	Parameter		Condition	MIN	TYP	MAX	Unit
IVD	Circuit Current		No Signal	TBD	28	TBD	mA
			MUTE	TBD	-	TBD	mA
			Stand-by	-	-	10	uA
VDPR	Detection Voltage		VD under-voltage	TBD	9.8	TBD	V
TPR	Protection Temperature		Thermal Shut-dawn	-	150	-	℃
TRL	Release Temperature		Thermal Shut-dawn	-	120	-	℃
IPR	Protection Current		Output over-current	-	6	-	A
Pomax	Maximum output power	at SE	THD=10%、VD=24V、RL=8Ω	TBD	10	-	W/ch
		at BTL	THD=10%、VD=18V、RL=8Ω	TBD	20	-	W
THD	Total Harmonic Distortion		Po=1W	-	0.1	TBD	%
No	Output Noise level		A-Weighted filter	-	(100)	TBD	uVrms
Eff	Power Efficiency	at SE	Po=10+10W	TBD	93	-	%
		at BTL	Po=20W	TBD	89	-	%
Mute	Mute Attenuation			TBD	80	-	dB
PSRR	Ripple Rejection Ratio		dVD=100mVrms,f=100 Hz	TBD	50	-	dB

9. Application Examples

(note)
"R for GND" 's are for the evaluation only and not needed actually.

Fig.4 SE operation mode(10Wx2ch)

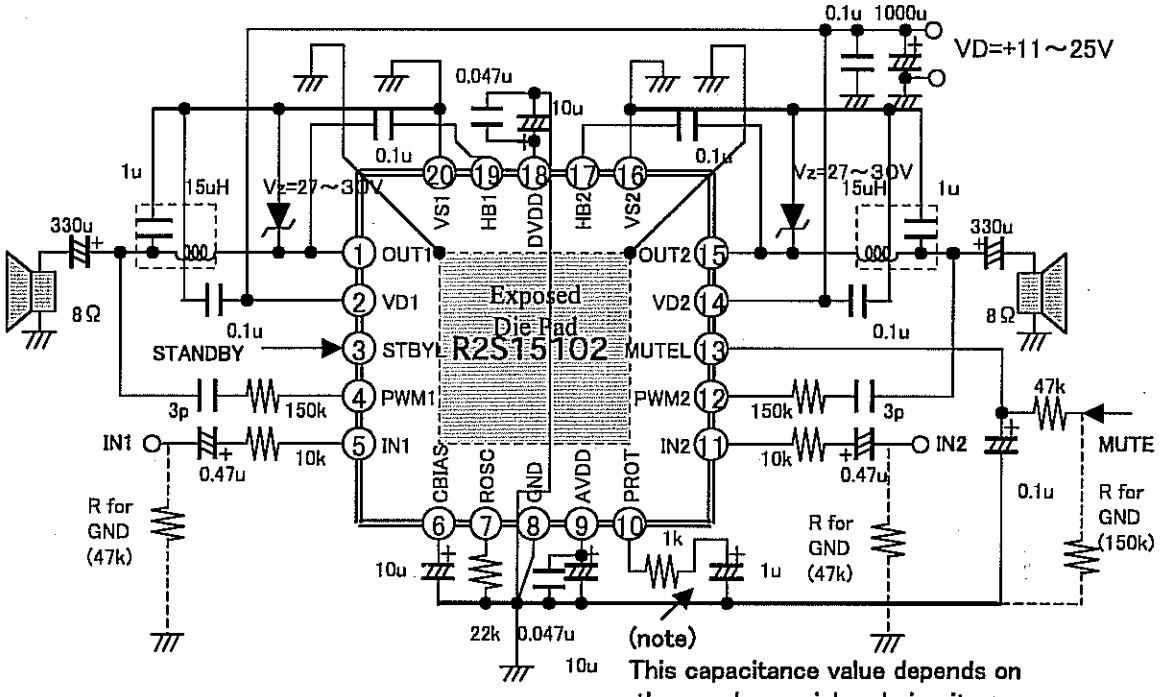


Fig.5 BTL operation mode (20W)

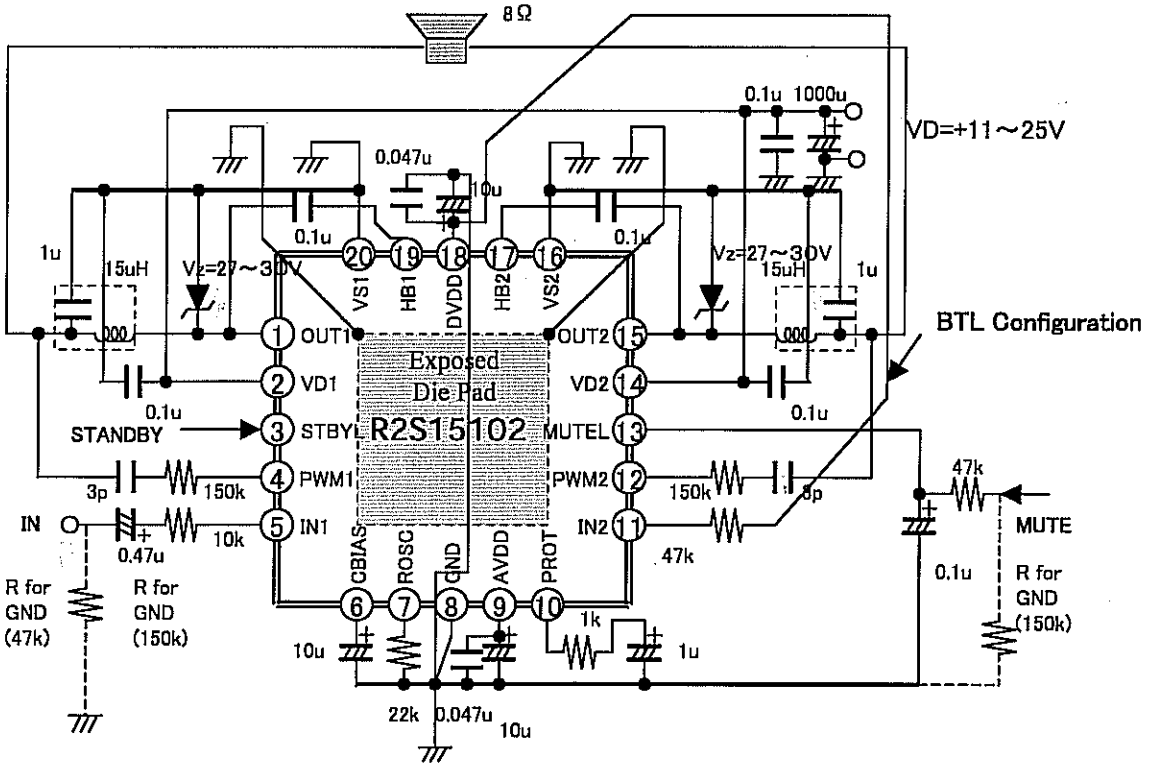
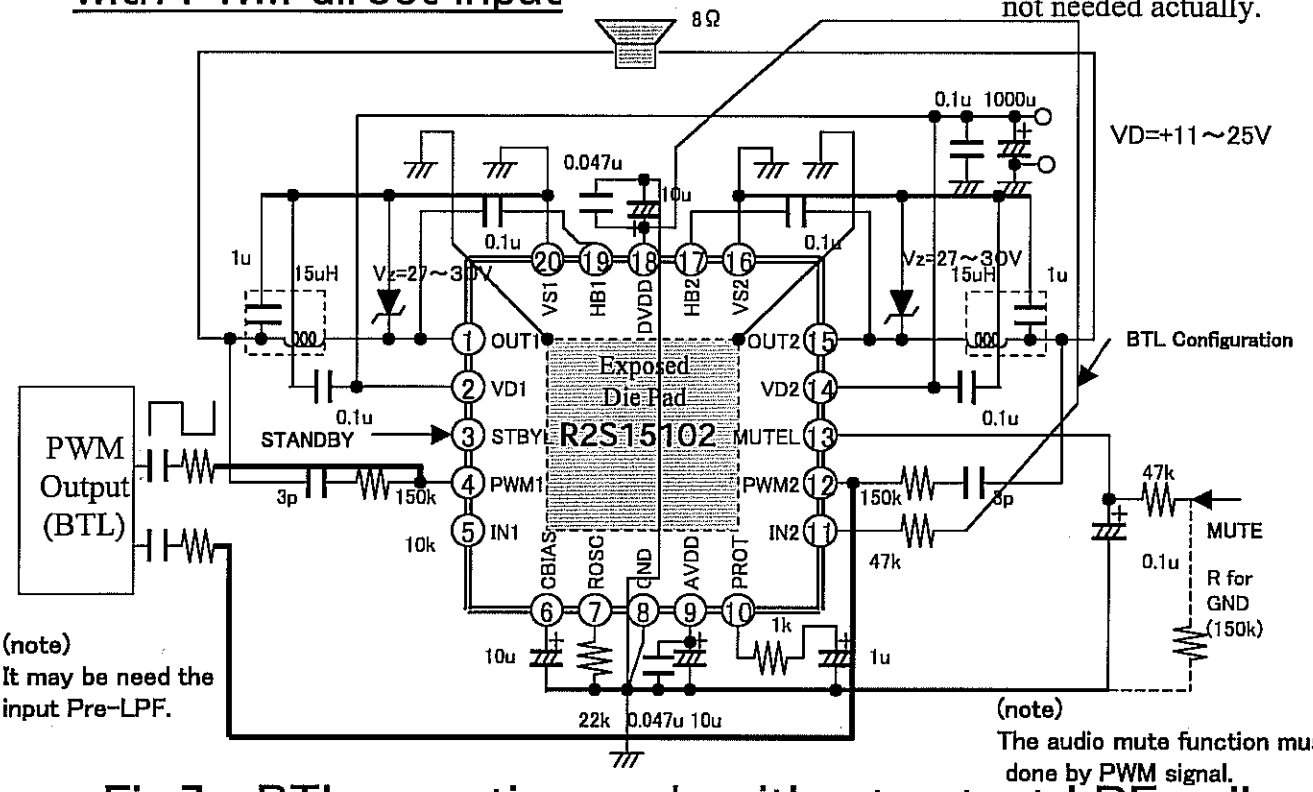


Fig.6 BTL operation mode(20W) with PWM direct input

(note)
"R for GND" 's are for the evaluation only and not needed actually.

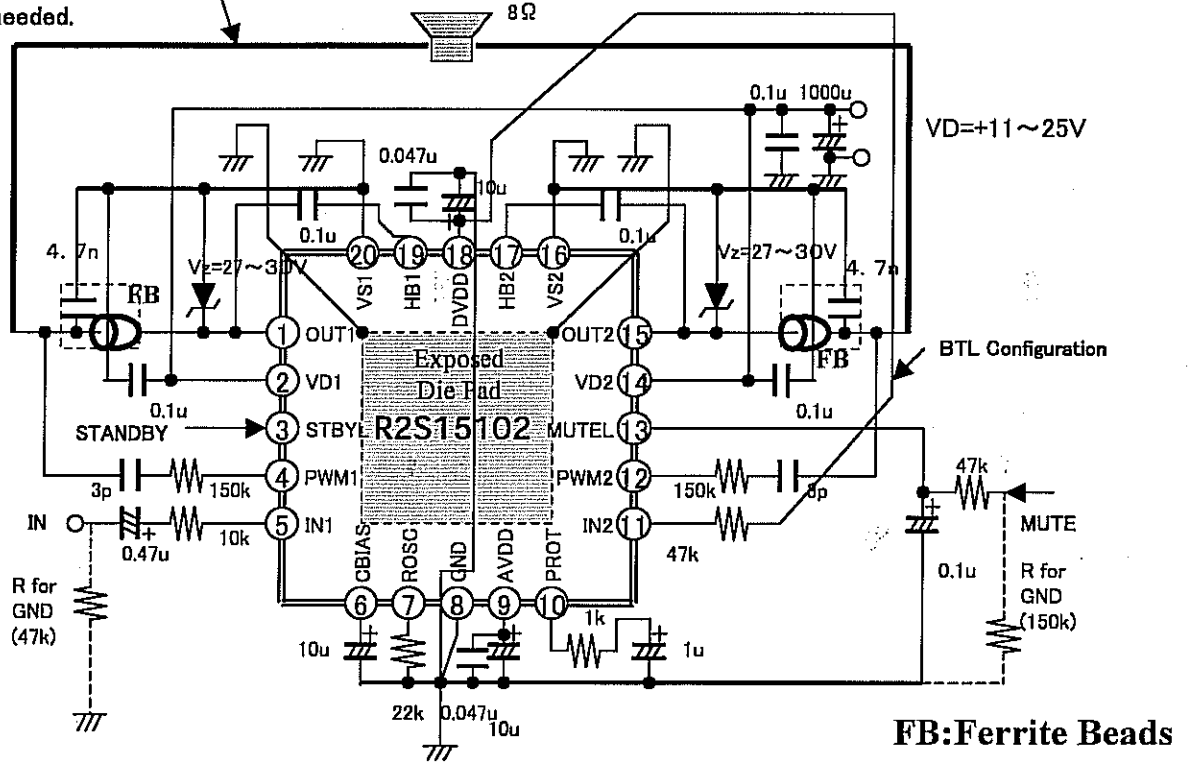


(note)
It may be need the input Pre-LPF.

(note)
The audio mute function must be done by PWM signal.

Fig.7 BTL operation mode without output LPF coil

If this speaker lines is very short, the LPF coil is not needed.



FB:Ferrite Beads

TFT LCD Approval Specification

MODEL NO.: V260B1 - L01

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V260B1- L01 is a TFT Liquid Crystal Display module with 12-CCFL Backlight unit and 1ch-LVDS interface. The display diagonal is 26". This module supports 1366 x 768 WXGA format and can display 16.2M colors(6-bits+FRC colors). The inverter module for backlight is built-in.

1.2 FEATURES

- Excellent brightness 500nits
- Contrast ratio 800:1
- Fast response time (8ms)
- Color saturation NTSC 72%
- WXGA (1366 x 768 pixels) resolution
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Viewing angle: 160(H)/150(V) (CR>10) TN technology
-Color reproduction (Nature color)
- RoHS compliance

1.3 APPLICATION

- TFT LCD TVs
- High brightness, multi-media displays

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	575.769 (H) x 323.712 (V) (26" diagonal)	mm	(1)
Bezel Opening Area	580.8 (H) x 328.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1366 x R.G.B. x 768	pixel	
Pixel Pitch (Sub Pixel)	0.1405 (H) x 0.4215 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	16.2M	color	
Display Operation Mode	Transmissive mode / Normally White	-	
Surface Treatment	Anti-Glare coating (Haze 25%) Hard coating (3H)	-	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	625	626	627	mm	
	Vertical(V)	372	373	374	mm	
	Depth(D)	35.6	36.6	37.6	mm	To PCB cover
	Depth(D)	41.2	42.2	43.2	mm	To inverter cover
Weight		--	4500	--	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

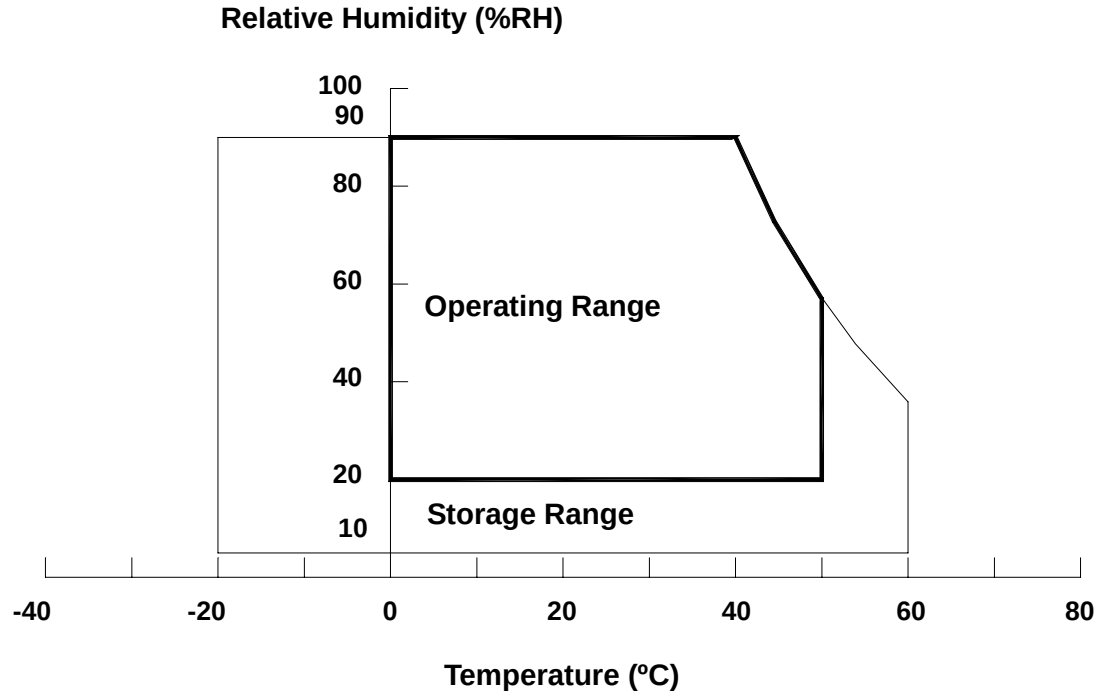
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 60 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 60 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 500 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	6.0	V	(1)
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Lamp Voltage	V_W	Ta = 25 ℃	—	—	3000	V_{RMS}	
Power Supply Voltage	V_{BL}	—	0	—	30	V	(1)
Control Signal Level	—	—	-0.3	—	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals includes Backlight On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

3. ELECTRICAL CHARACTERISTICS

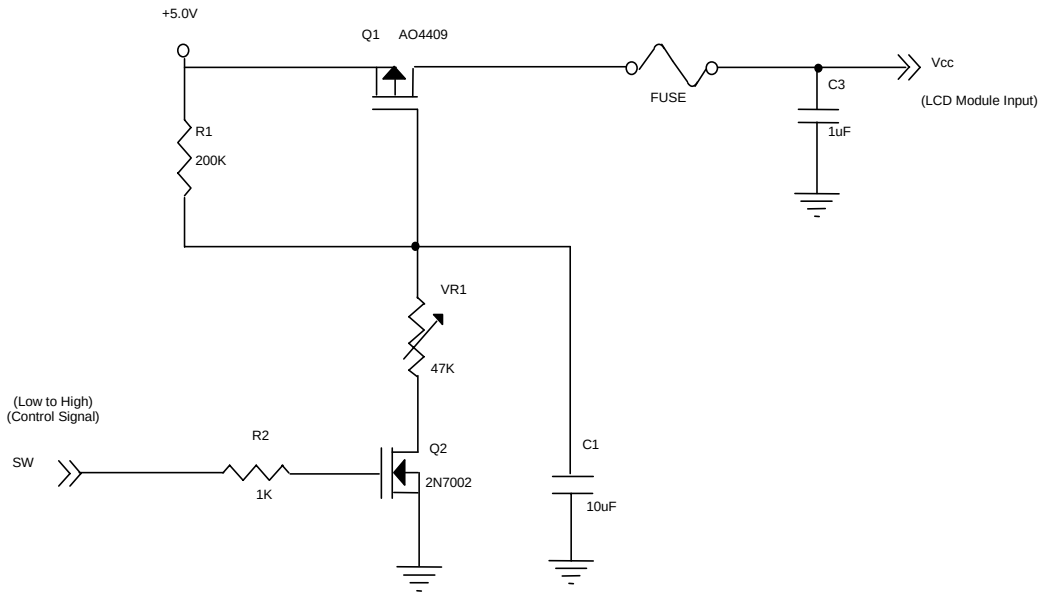
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

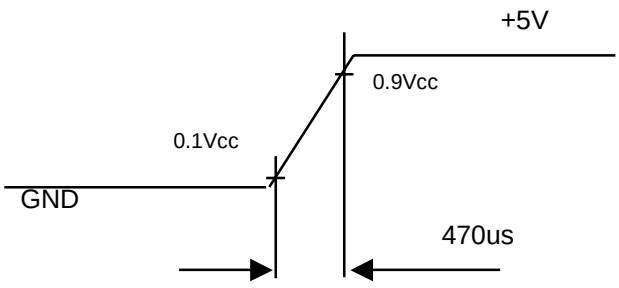
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	4.5	5.0	5.5	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	100	mV	
Rush Current		I_{RUSH}	-	-	3.0	A	(2)
Power Supply Current	White	I_{CC}	-	0.6	-	A	(3)
	Black		-	1.0	1.3	A	
	Vertical Stripe		-	0.9	-	A	
LVDS Interface	Differential Input High Threshold Voltage	V_{LVTH}	-	-	+100	mV	
	Differential Input Low Threshold Voltage	V_{LVTL}	-100	-	-	mV	
	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T		100		ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 5 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

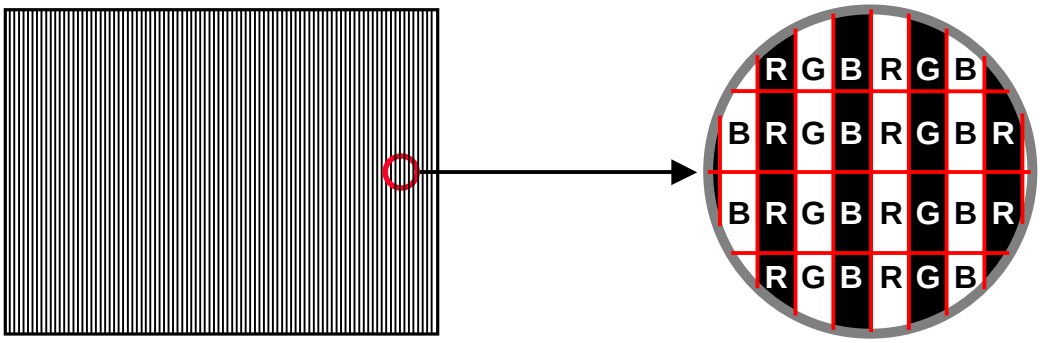
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT INVERTER UNIT

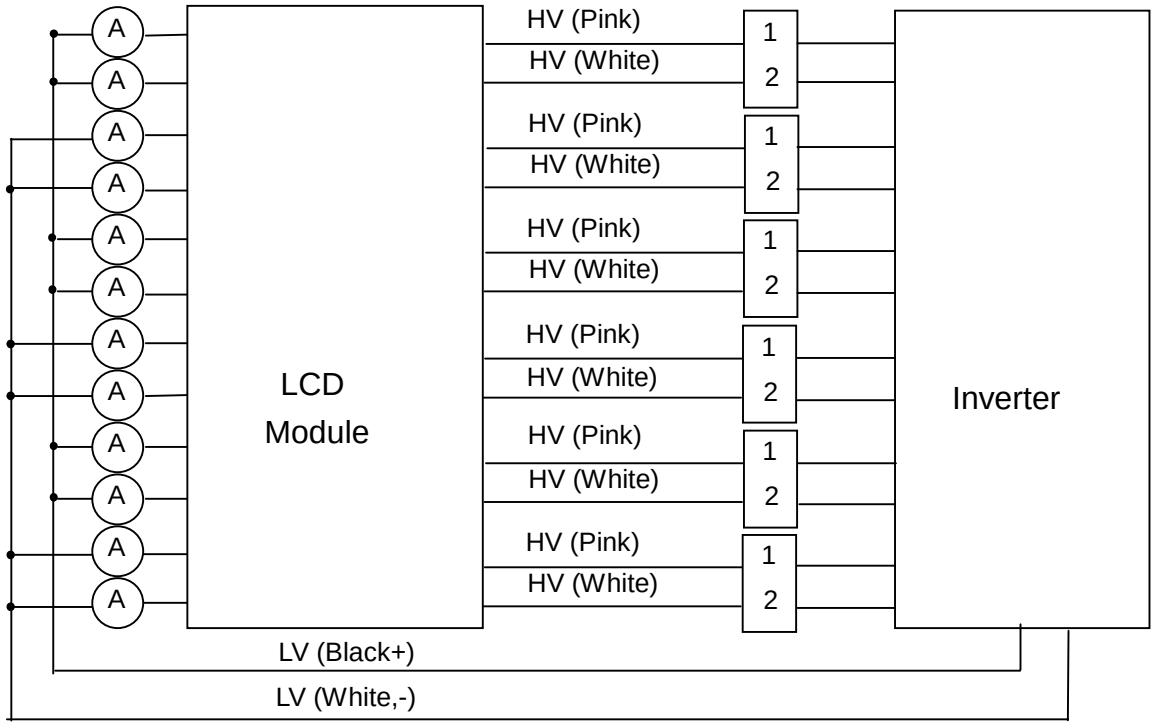
3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	V_W	-	970	-	V_{RMS}	I_L = 5.0mA
Lamp Current	I_L	4.5	5.0	5.5	mA_{RMS}	(1)
Lamp Starting Voltage	V_S	-	-	1650	V_{RMS}	(2), Ta = 0 ºC
		-	-	1500	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_O	40	-	80	KHz	(3)
Lamp Life Time	L_{BL}	50,000	60,000	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	66	69	W	(5)(6), I_L = 5.0mA
Power Supply Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Power Supply Current	I_{BL}	-	2.75	-	A	Non Dimming
Input Ripple Noise	-	-	-	500	mV_{P-P}	V_{BL} =22.8V
Backlight Turn on Voltage	V_{BS}	1650	-	-	V_{RMS}	Ta = 0 ºC
		1500	-	-	V_{RMS}	Ta = 25 ºC
Oscillating Frequency	F_W	55	58	61	kHz	
Dimming Frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second under starting up duration. Otherwise the lamp could not be lighted on completed.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point.) as the time in which it continues to operate under the condition Ta = 25 ±2°C and I_L = 4.5~ 5.5mA_{RMS}.

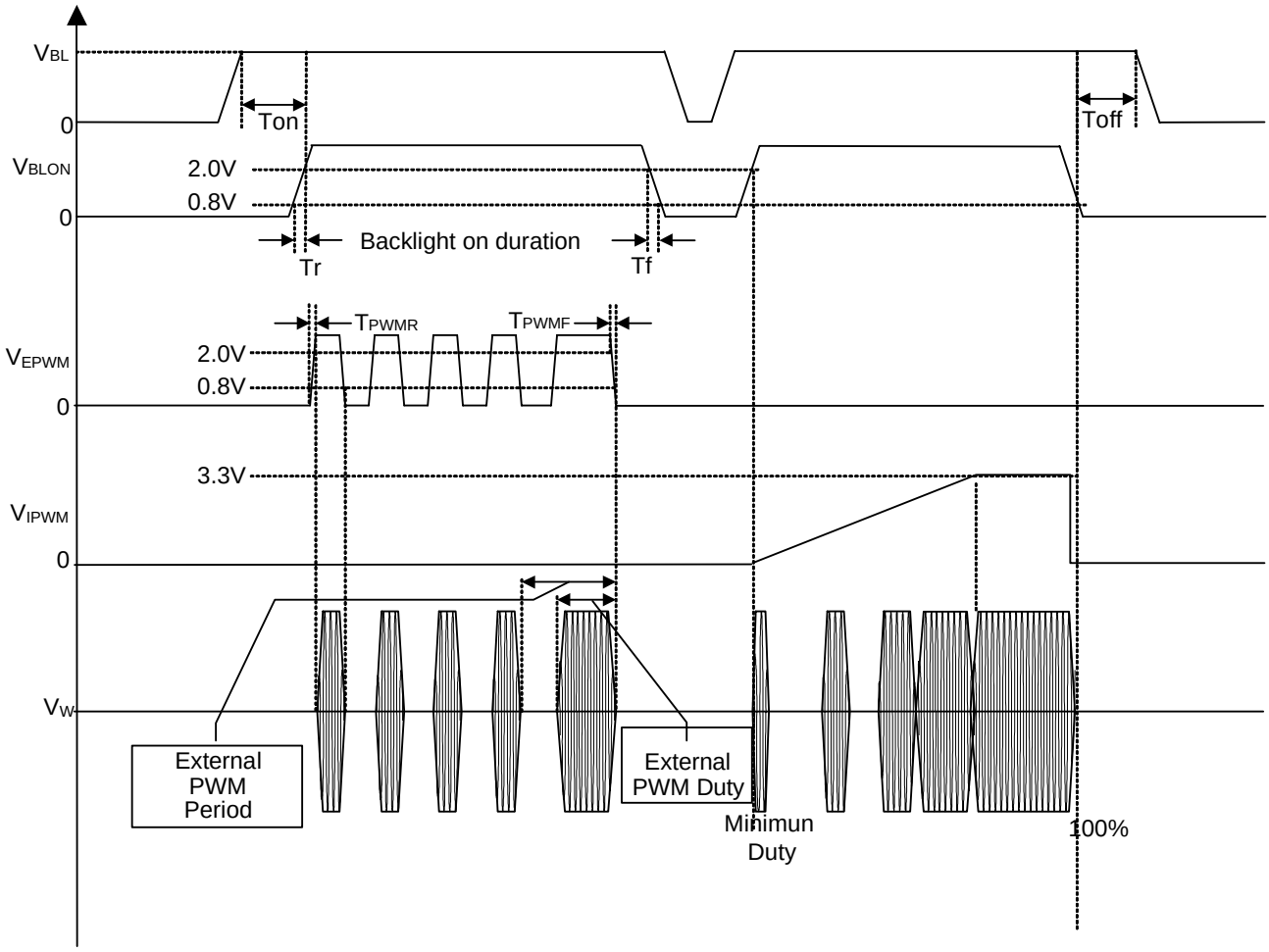
Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement of Max. value is based on 26" backlight unit under 24V input voltage and 6.3mA lamp in average after lighting for 30 minutes.

3.2.3 INVERTER INTERTFACE CHARACTERISTICS

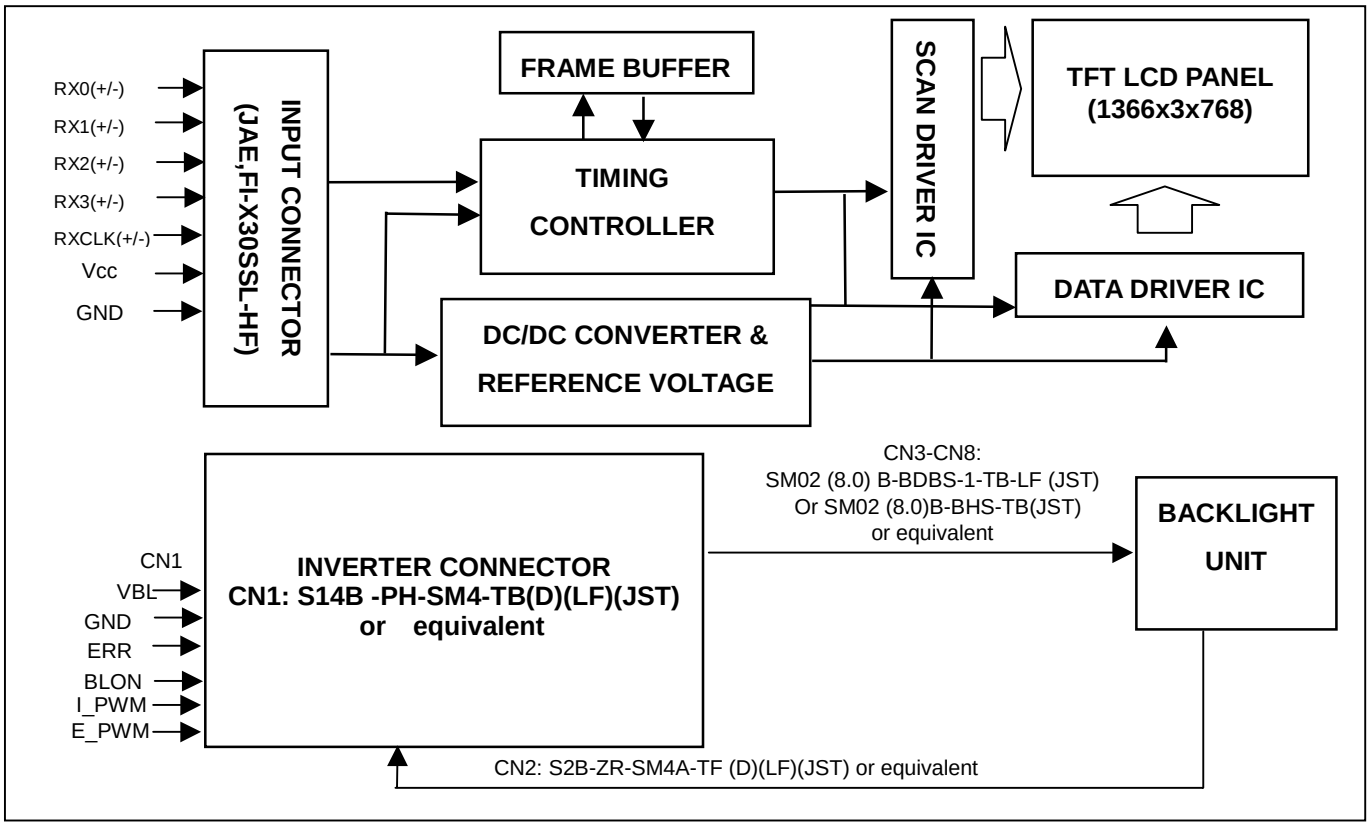
Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Error Signal		ERR	—	—	—	—	—	(Note 1)
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	V_{SEL} = L	3.0	3.15	3.3	V	Maximum duty ratio
	MIN			—	0	—	V	Minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	V_{SEL} = H	2.0	—	5.0	V	duty on
	LO			0	—	0.8	V	duty off
Control Signal Rising Time		T_r	—	—	—	100	ms	
Control Signal Falling Time		T_f	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
BLON Delay Time		T_{on}	—	1	—	—	ms	
BLON Off Time		T_{off}	—	1	—	—	ms	

Note (1) When inverter protective function is triggered, ERR will output open collector status. In normal operation, the signal of ERR will output a low level voltage.


VBL
0
Ton
Toff
VBLON
2.0V
0.8V
0
Backlight on duration
Tr
Tf
TPWMR
TPWMF
VEPWM
2.0V
0.8V
0
3.3V
VIPWM
0
VW
External PWM Period
External PWM Duty
Minimun Duty
100%

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	NC	No Connection	(3)
2	NC	No Connection	(3)
3	NC	No Connection	(3)
4	GND	Ground	
5	RX0-	Negative transmission data of pixel 0	
6	RX0+	Positive transmission data of pixel 0	
7	GND	Ground	
8	RX1-	Negative transmission data of pixel 1	
9	RX1+	Positive transmission data of pixel 1	
10	GND	Ground	
11	RX2-	Negative transmission data of pixel 2	
12	RX2+	Positive transmission data of pixel 2	
13	GND	Ground	
14	RXCLK-	Negative of clock	
15	RXCLK+	Positive of clock	
16	GND	Ground	
17	RX3-	Negative transmission data of pixel 3	
18	RX3+	Positive transmission data of pixel 3	
19	GND	Ground	
20	NC	No Connection	
21	SELLVDS	Select LVDS data format	(2)
22	NC	No Connection	(3)
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	VCC	Power supply: +5V	
27	VCC	Power supply: +5V	
28	VCC	Power supply: +5V	
29	VCC	Power supply: +5V	
30	VCC	Power supply: +5V	

Note (1) Connector Part No.: JAE,FI-X30SSL-HF or compatible

Note (2) High: Normal, Ground or OPEN: JEIDA LVDS format

Please refer to 5.5 LVDS INTERFACE (Page 17)

Note (3) Reserved for internal use. Please leave it open.

5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN3-CN8 (Housing): BDBR-03(4.0)V-1S (JST) or BHR-03VS-1(JST) or equivalent.

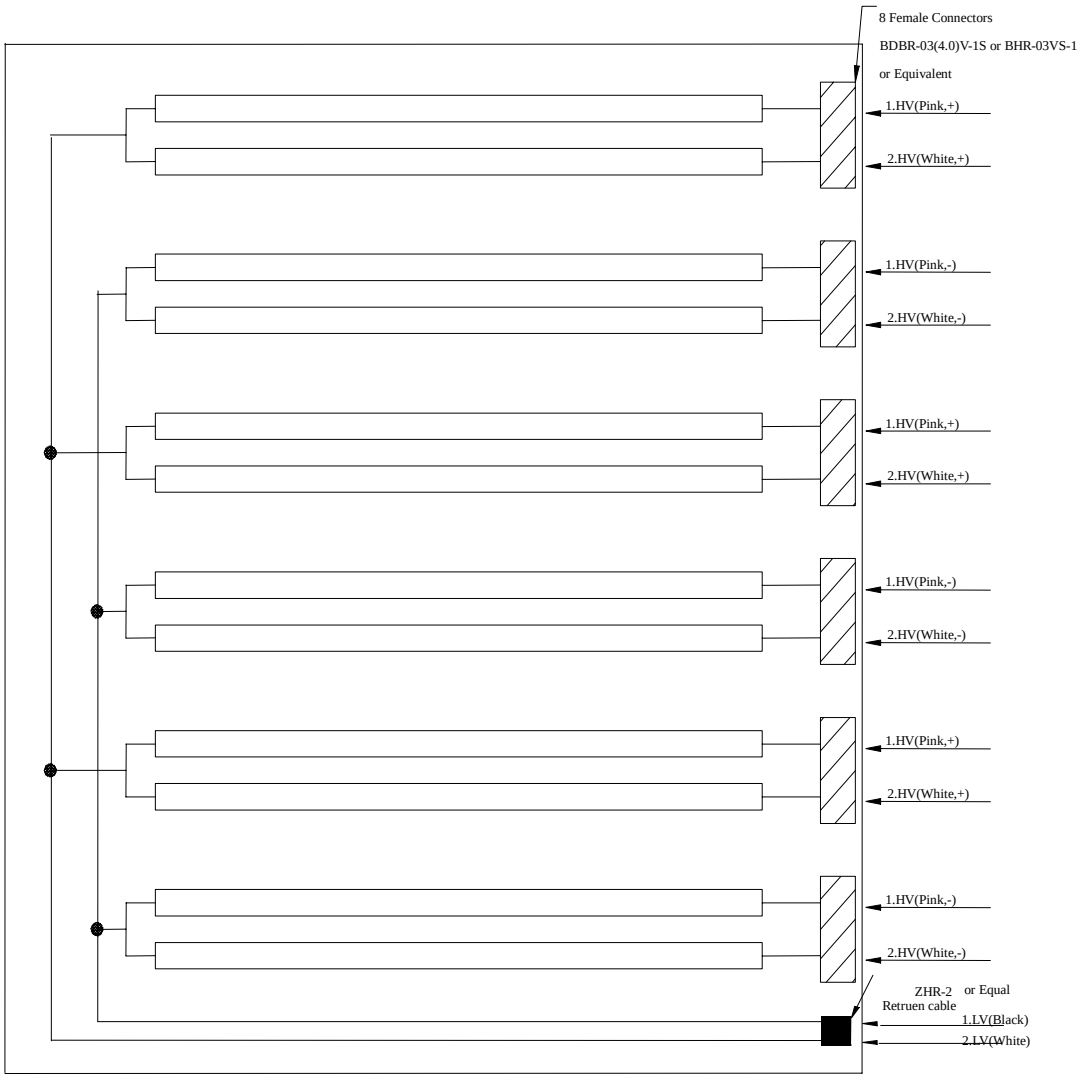
Pin No.	Symbol	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BDBR-03 (4.0)V-1S(JST),or BHR-03VS-1(JST)or equivalent. The mating header on inverter part number is SM02(8.0)B-BDBS-1-TB-LF(JST)or SM02(8.0)B-BHS-TB(JST) or equivalent.

CN2 (Housing): ZHR-2 (JST) or equivalent

Pin No.	Symbol	Description	Wire Color
1	LV	Low Voltage (+)	Black
2	LV	Low Voltage (-)	White

Note (2) The backlight interface housing and return cable for low voltage side is a model ZHR-2 , manufactured by JST or equivalent. The mating header on inverter part number is S2B-ZR-SM4A-TF(D)(LF) or equivalent.



5.3 INVERTER UNIT

CN1(Header): S14B -PH-SM4-TB(D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal(Open collector)
12	BLON	BL ON/OFF
13	I_PWM	Internal PWM Control
14	E_PWM	External PWM Control

Notice:

#PIN 13:Analog Dimming Control (Use Pin 13) : 0V~3.3V and Pin 14 must open.

#PIN 14:PWM Dimming Control (Use Pin 14) : Pin 13 must open.

#Pin 13(I_PWM) and Pin 14(E_PWM) can not open in same period.

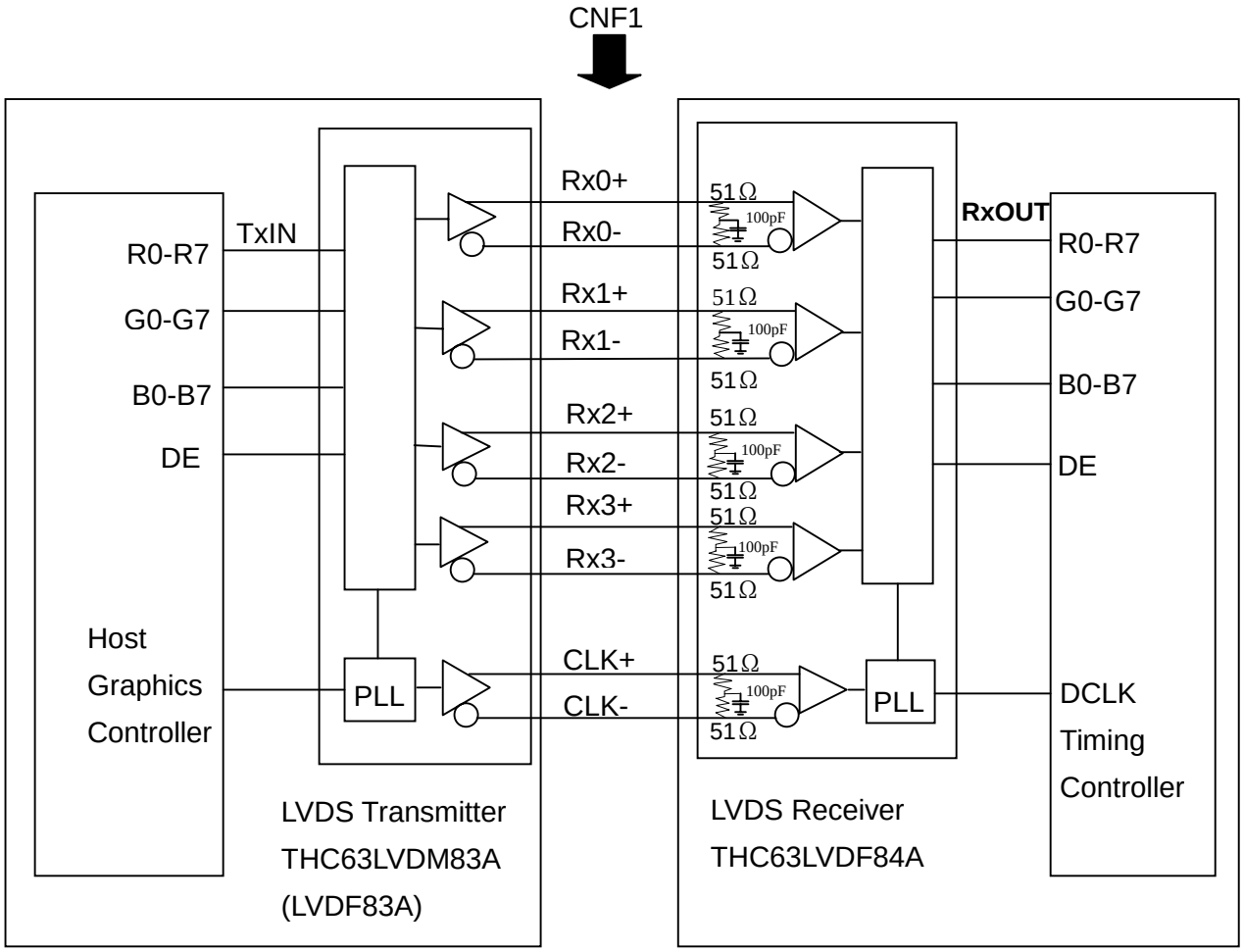
CN2(Header): S2B-ZR-SM4A-TF or equivalent.

Pin No.	Symbol	Description
1	CCFL COLD	CCFL low voltage (+)
2	CCFL COLD	CCFL low voltage (-)

CN3-CN8 (Header): SM02(8.0)B-BDBS-1-TB-LF(JST) or SM02(8.0)B-BHS-TB or equivalent.

Pin	Name	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

5.4 BLOCK DIAGRAM OF INTERFACE



R0~R7 : Pixel R Data ,

G0~G7 : Pixel G Data ,

B0~B7 : Pixel B Data ,

DE : Data enable signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

	SIGNAL		TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
	SELLVDS =H	SELLVDS= L or OPEN	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	SELLVDS =H	SELLVDS =L or OPEN
24 bit	R0	R2	51	TxIN0			27	Rx OUT0	R0	R2
	R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
	R2	R4	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2	R4
	R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
	R4	R6	56	TxIN4			33	Rx OUT4	R4	R6
	R5	R7	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5	R7
	G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
	G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
	G2	G4	7	TxIN9			39	Rx OUT9	G2	G4
	G3	G5	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3	G5
	G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
	G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
	B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
	B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
	B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
	B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
	B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
	B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
	DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
	R6	R0	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6	R0
	R7	R1	2	TxIN5			34	Rx OUT5	R7	R1
	G6	G0	8	TxIN10			41	Rx OUT10	G6	G0
	G7	G1	10	TxIN11			42	Rx OUT11	G7	G1
	B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
	B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
	RSVD 1	RSVD 1	25	TxIN23			2	Rx OUT23	NC	NC
	RSVD 2	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	NC	NC
	RSVD 3	RSVD 3	28	TxIN25			5	Rx OUT25	NC	NC
		DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK	

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE: Data enable signal

Notes(1) RSVD(reserved)pins on the transmitter shall be “H” or “L”.

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

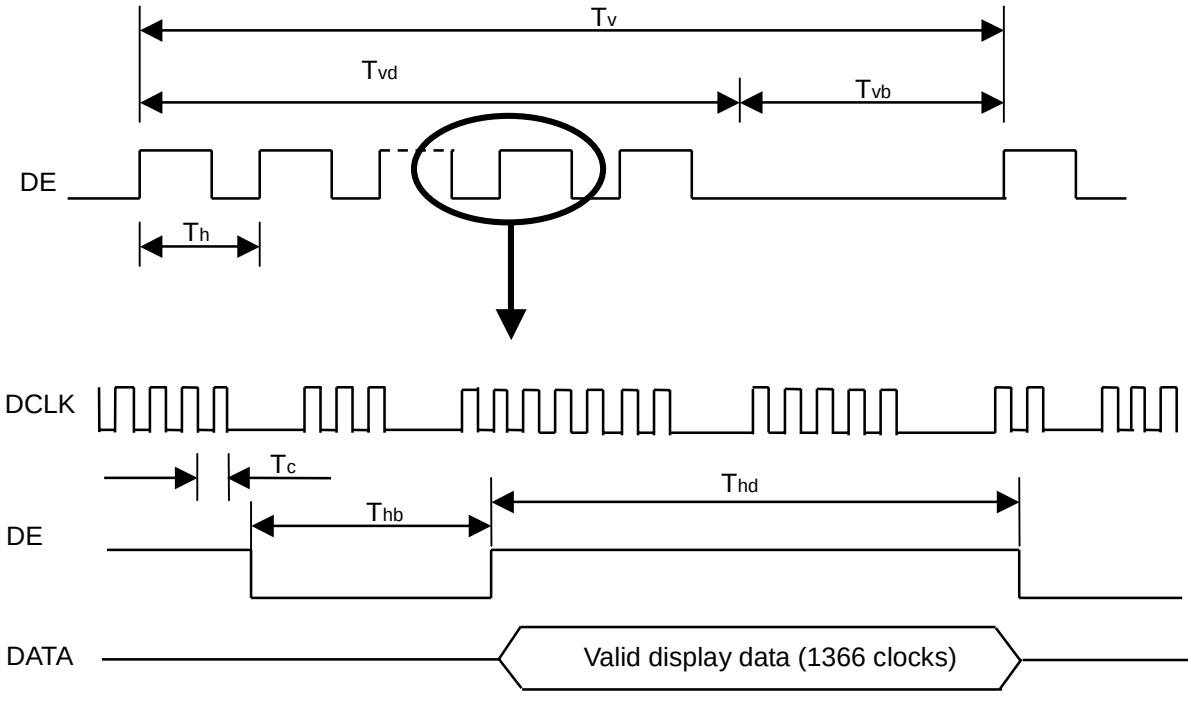
The input signal timing specifications are shown as the following table and timing diagram**.**

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74	82	MHz	
	Input cycle to cycle jitter	Trcl	-	-	200	ps	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr_5	47	50	53	Hz	(2)
		Fr_6	57	60	63	Hz	
	Total	Tv	778	795	888	Th	Tv=Tvd+Tvb
	Display	Tvd	768	768	768	Th	-
	Blank	Tvb	10	27	120	Th	-
Horizontal Active Display Term	Total	Th	1442	1572	1936	Tc	Th=Thd+Thb
	Display	Thd	1366	1366	1366	Tc	-
	Blank	Thb	76	206	570	Tc	-

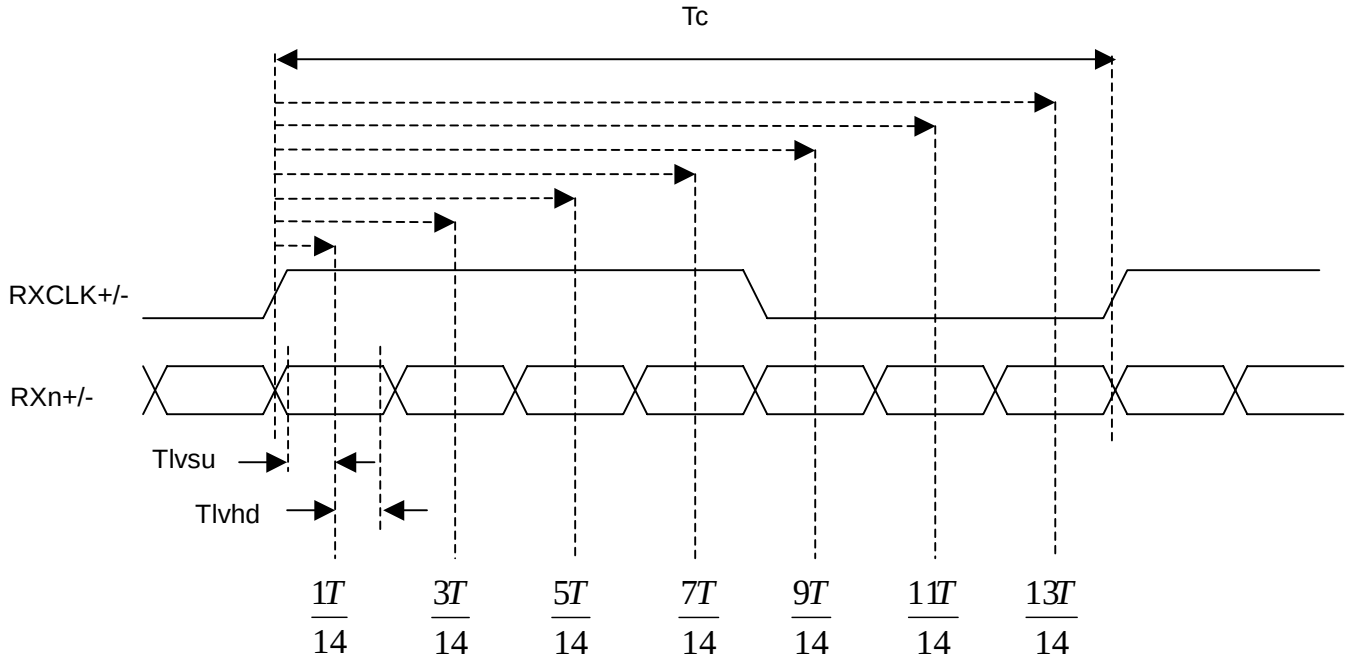
Note (1) Since this module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

(2) Please refer to 5.1 for detail information.

INPUT SIGNAL TIMING DIAGRAM

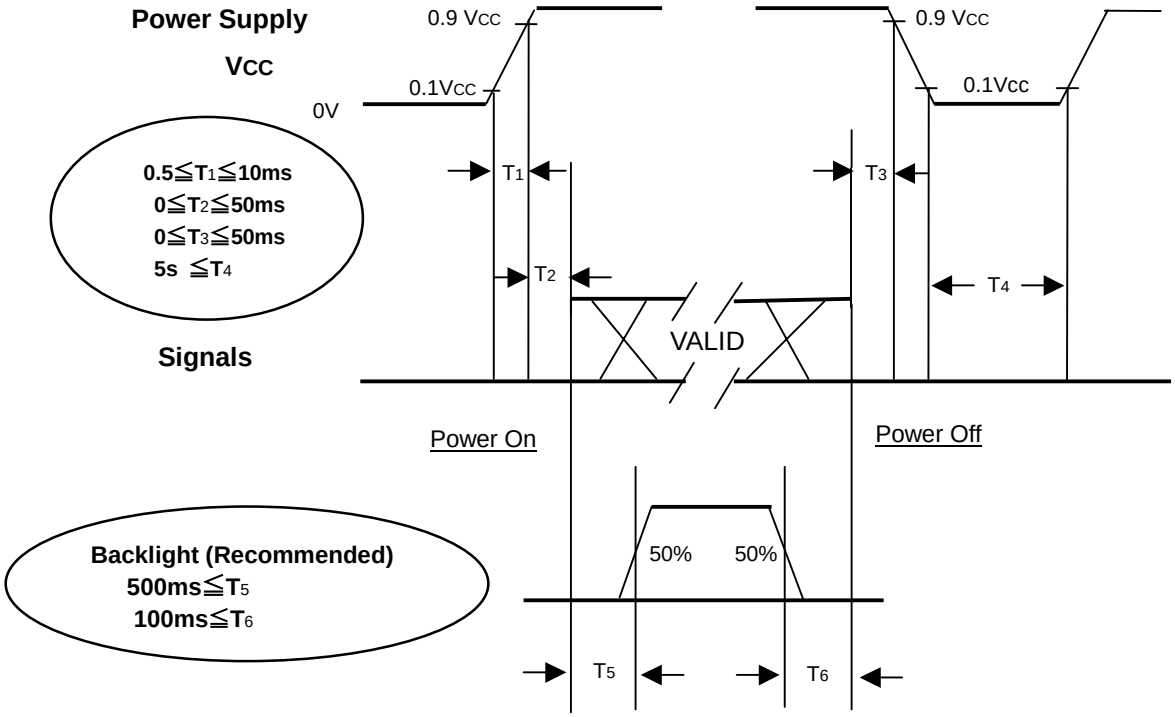


LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	5.0 ± 0.5	mA
Oscillating Frequency (Inverter)	F_W	58 ± 3	KHz
Vertical Frame Rate	Fr	60	Hz

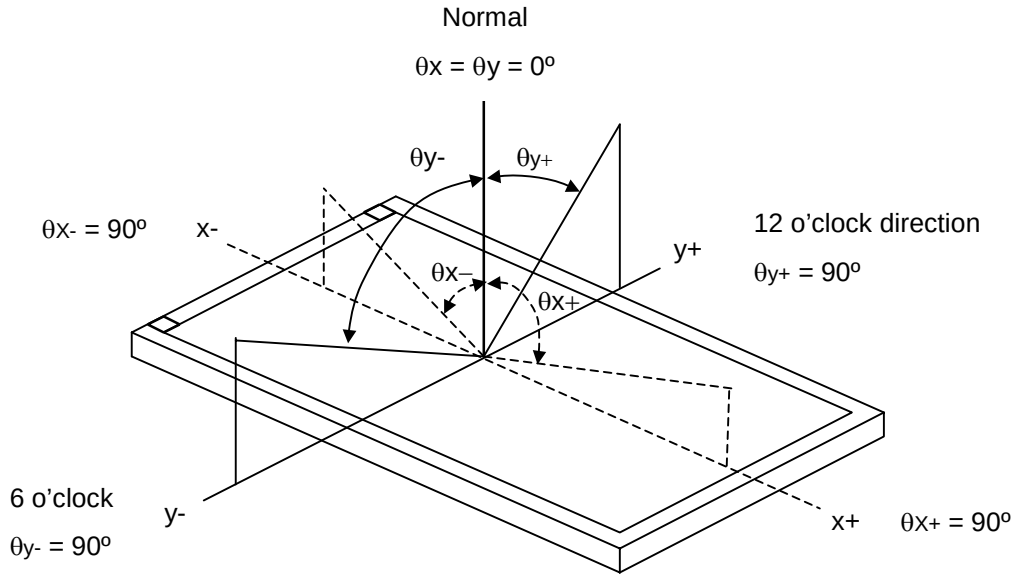
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	600	800		-	(2)
Response Time		T_R			3	5	ms	(3)
		T_F			5	8		
Center Luminance of White		L_C		400	500			(4)
White Variation		δW				1.3	-	(7)
Cross Talk		CT				4	%	(5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.637	Typ. +0.03	-	(6)
		Ry			0.332		-	
	Green	Gx			0.268		-	
		Gy			0.590		-	
	Blue	Bx			0.150		-	
		By			0.059		-	
	White	Wx			0.280		Target	
		Wy			0.285			
	Color Gamut	CG		68	72		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥10	70	80		Deg.	(1)
		θ_x-		70	80			
	Vertical	θ_Y+		70	80			
		θ_Y-		60	70			

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

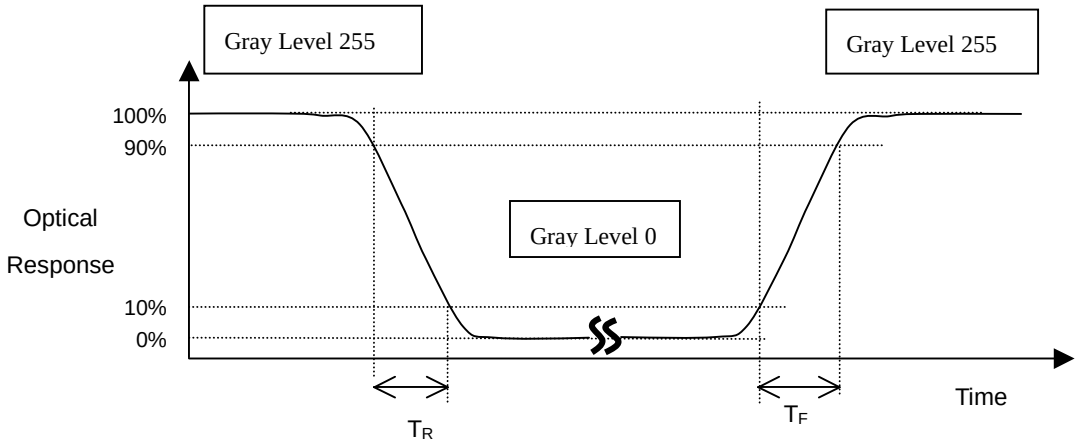
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (7).

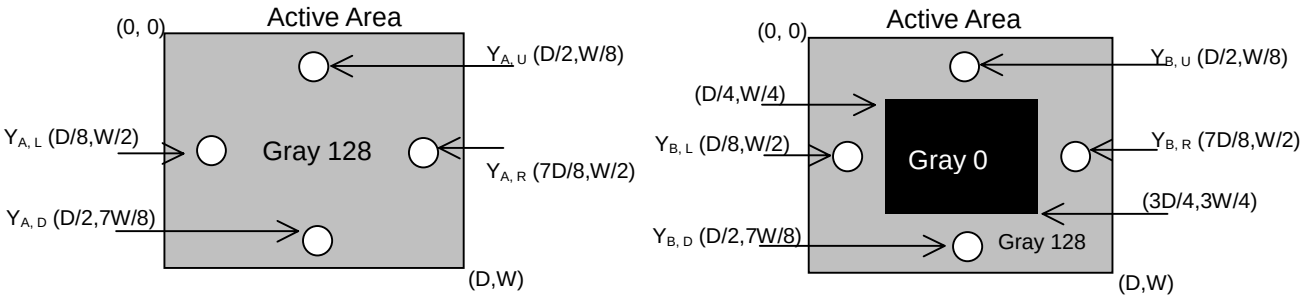
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

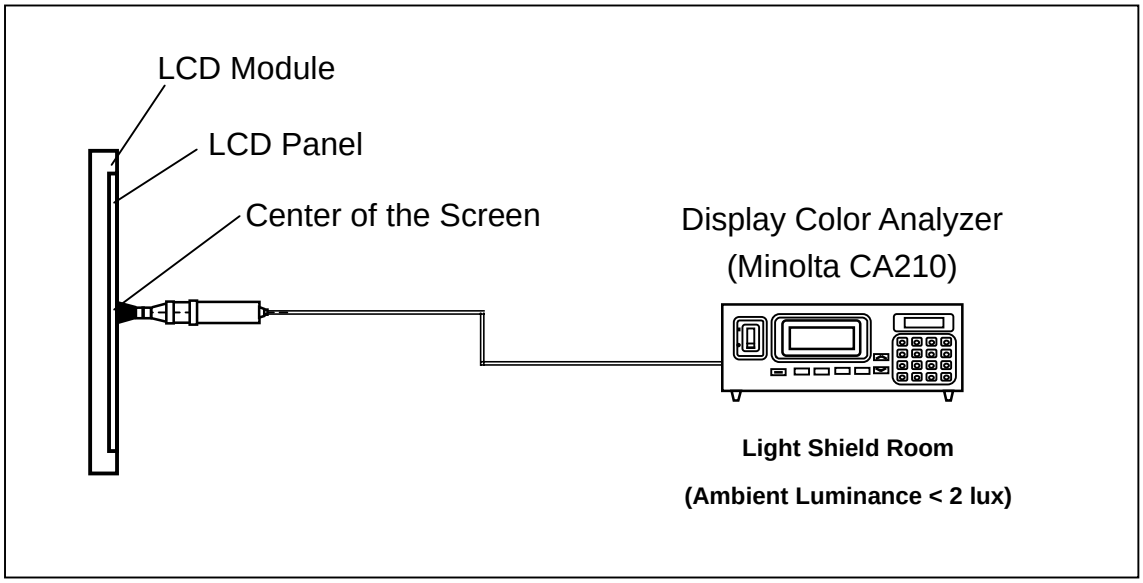
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

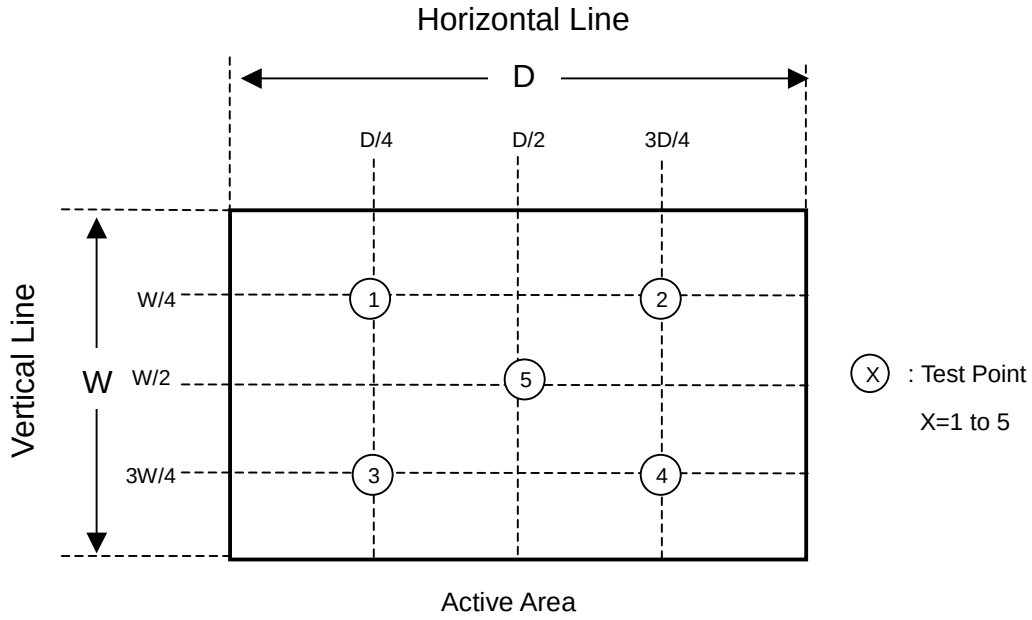
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

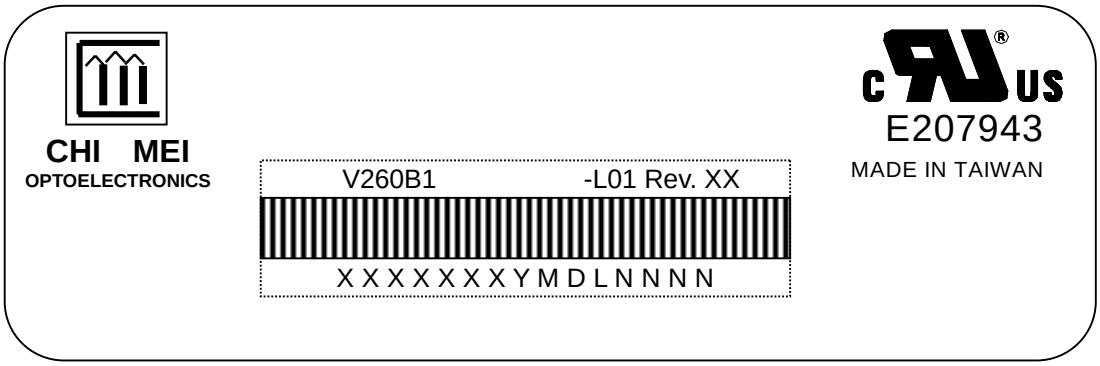
δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

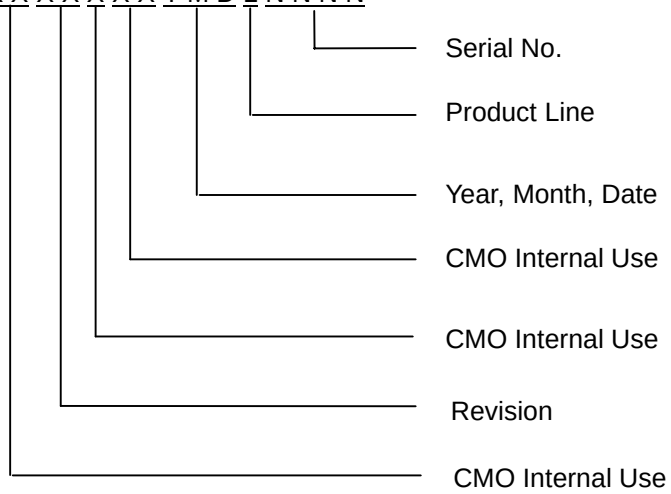
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V260B1-L01

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 5 LCD TV Modules / Carton

(2) Carton Dimensions : 742(L) X 399 (W) X 480 (H)

(3) Weight : Approximately 25.7Kg (5 Modules Per Carton)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

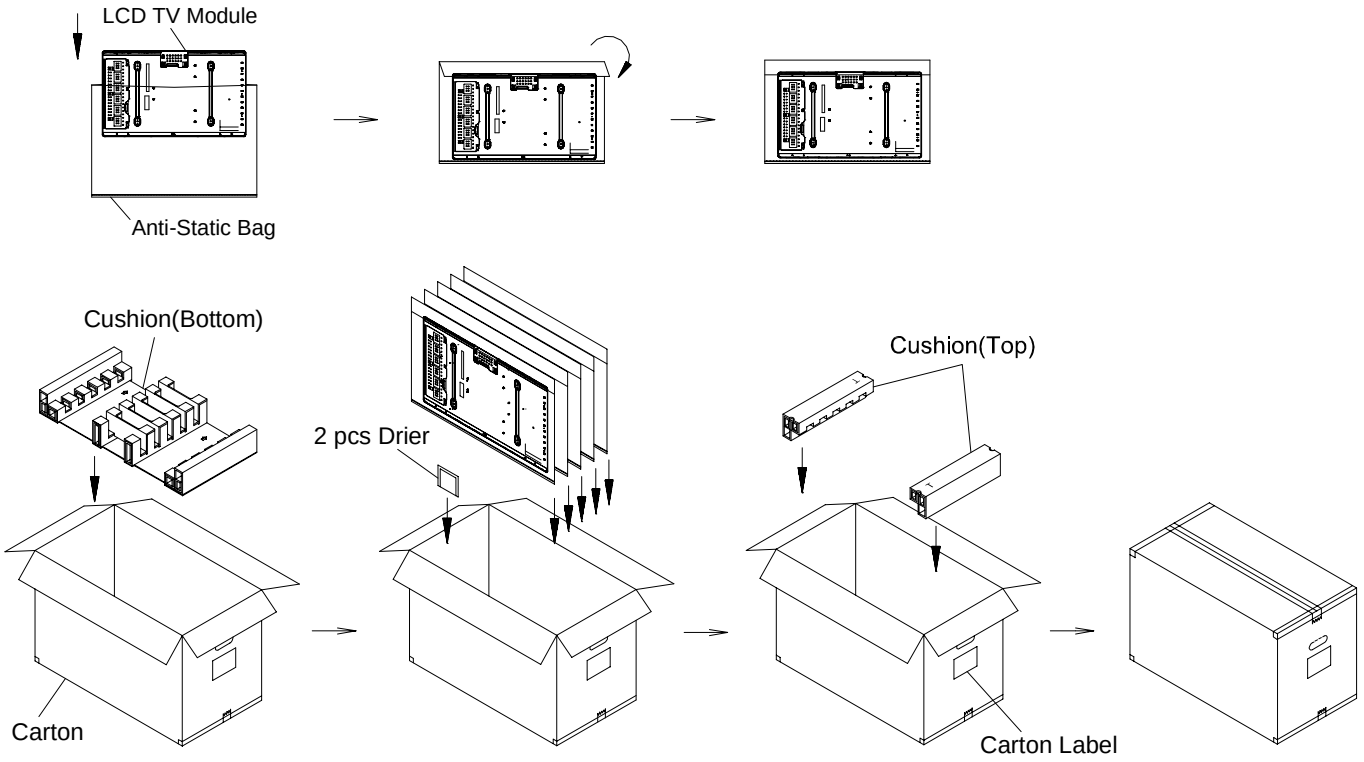
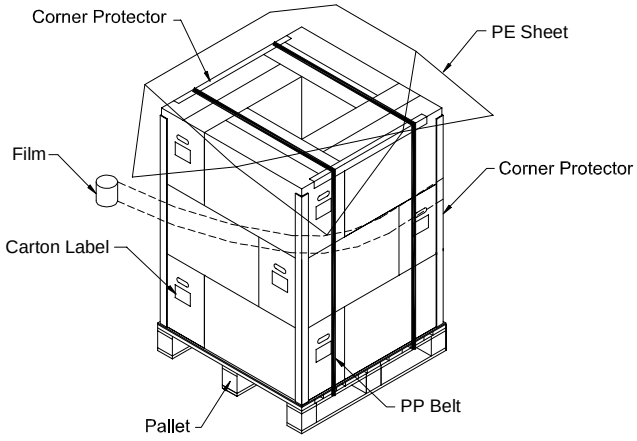


Figure.9-1 packing method

Air Transportation

Corner Protector:L1400*50*50mm
Corner Protector:L1130*50*50mm
Pallet:L1150*W1150*H140mm
Pallet Stack:L1150*W1150*H1580mm
Gross:323kg



Sea Transportation

Corner Protector:L1850*50*50mm
L11300*50*50mm
Pallet:L1150*W1150*H140mm
Pallet Stack:L1150*W1150*H2060mm
Gross:426kg

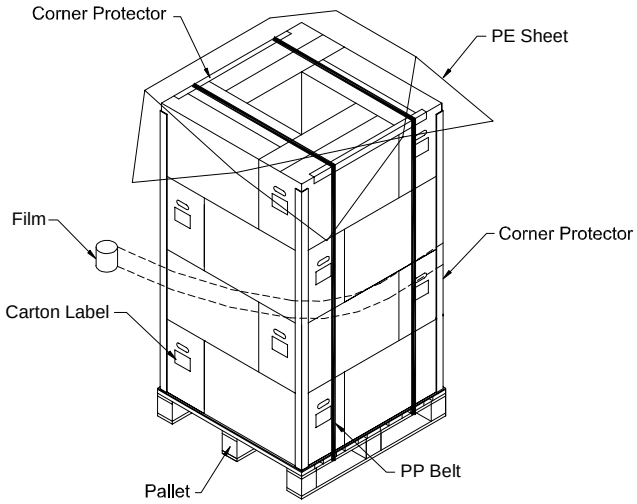


Figure. 9-2 packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

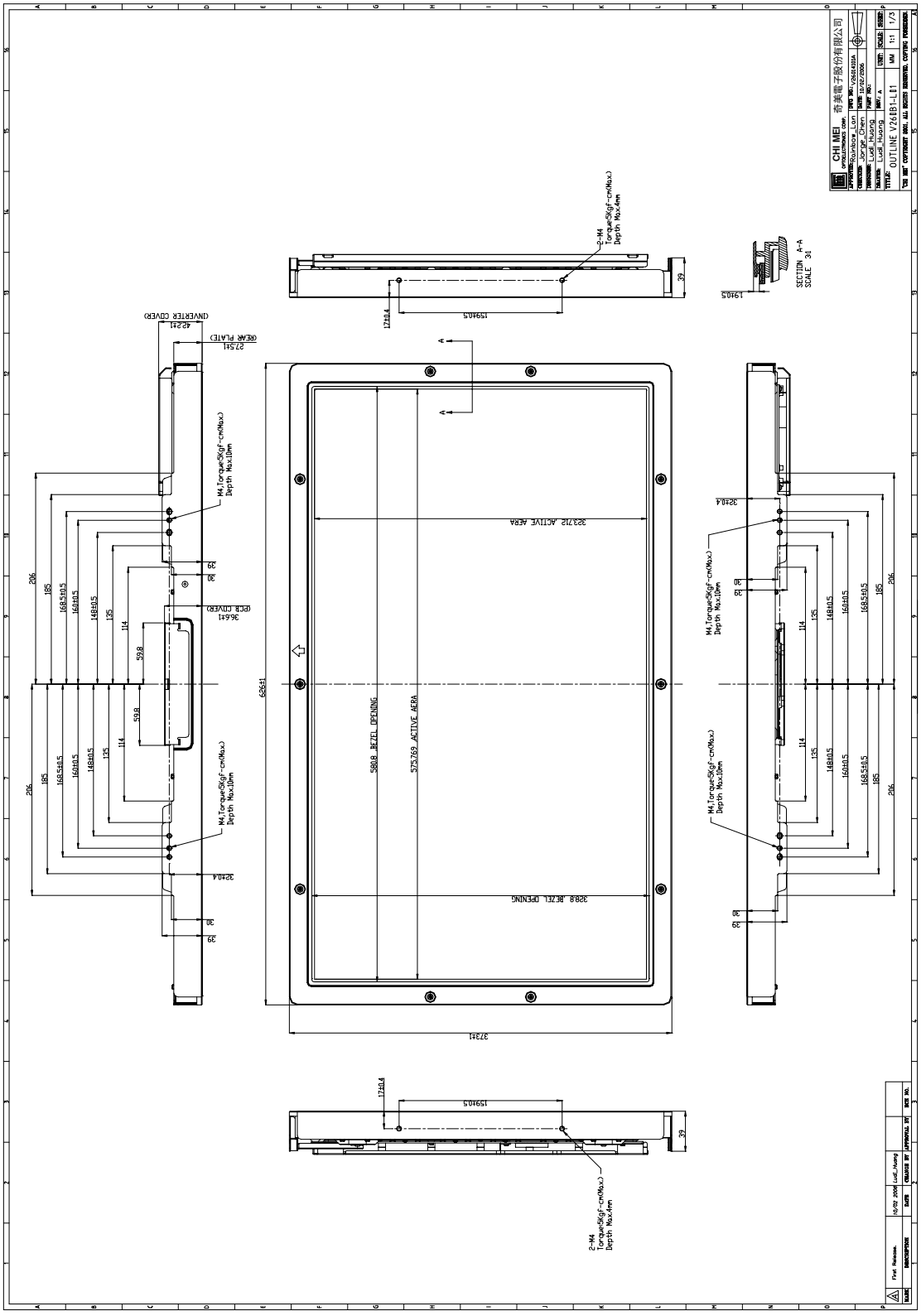
10.3 STORAGE PRECAUTIONS

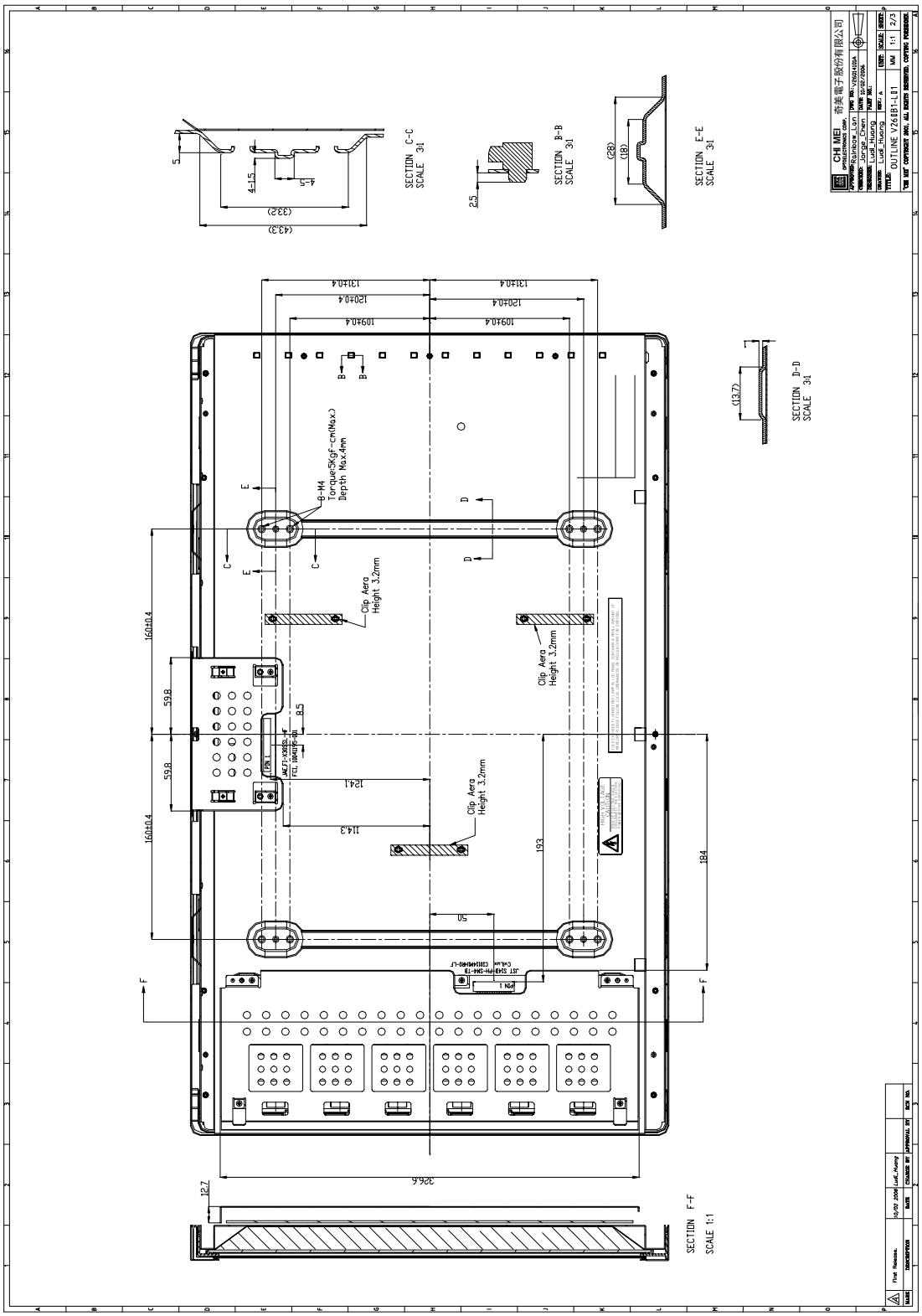
When storing modules as spares for a long time, the following precaution is necessary.

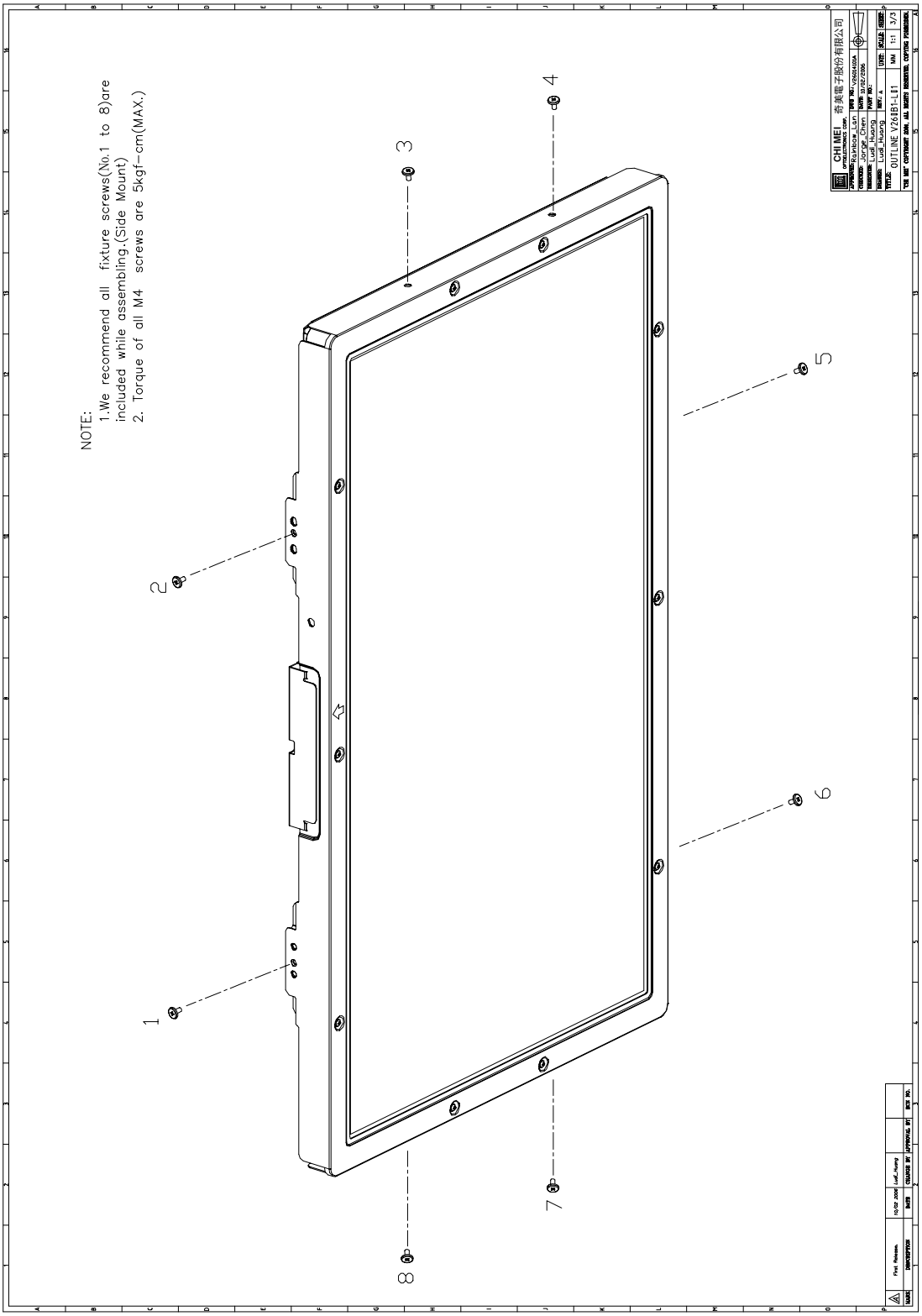
(1) Do not leave the module in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

(2) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

11. MECHANICAL CHARACTERISTICS

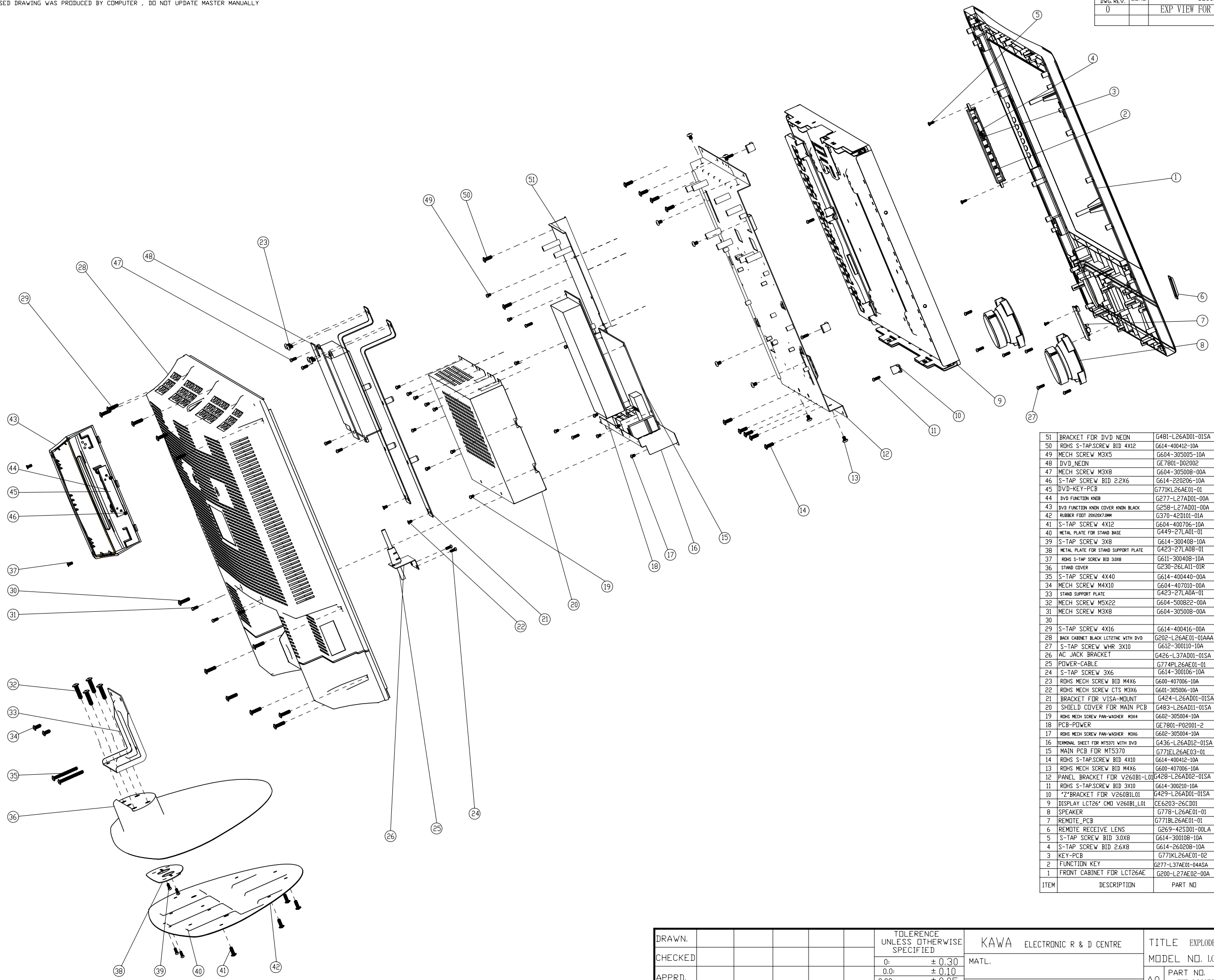



SECTION C-C
SCALE 3/1
SECTION B-B
SCALE 3/1
SECTION E-E
SCALE 3/1
SECTION D-D
SCALE 3/1
SECTION F-F
SCALE 1:1
Clip Area
Height 3.2mm
CHI MEI
OUTLINE V26B1-L01


NOTE:
1.We recommend all fixture screws(No.1 to 8)are included while assembling.(Side Mount)
2. Torque of all M4 screws are 5kgf-cm(MAX.)
1
2
3
4
5
6
7
8
CHI MEI
TITLE: OUTLINE V260B1-L01
SIZE: A1
SCALE: 1:1
SHEET: 3/3

NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER , DO NOT UPDATE MASTER MANUALLY

DWG.REV.	ZONE	DESCRIPTION	DATE	REVISOR
0		EXP VIEW FOR ASSY	10/3/07	QHY



ITEM	DESCRIPTION	PART NO	QTY.	REMARK
51	BRACKET FOR DVD NEON	G481-L26AD01-01SA	1	
50	ROHS S-TAP,SCREW BID 4X12	G614-400412-10A	2	
49	MECH SCREW M3X5	G604-305005-10A	2	
48	DVD_NEON	GE7801-D02002	1	
47	MECH SCREW M3X8	G604-305008-00A	4	
46	S-TAP SCREW BID 2.2X6	G614-220206-10A	2	
45	DVD-KEY-PCB	G771KL26AE01-01	1	
44	DVD FUNCTION KNOB	G277-L27AD01-00A	1	
43	DVD FUNCTION KNOB COVER KNOB BLACK	G258-L27AD01-00A	1	
42	RUBBER FOOT 20X20X7.0MM	G370-42D101-01A	4	
41	S-TAP SCREW 4X12	G604-400706-10A	6	
40	METAL PLATE FOR STAND BASE	G449-27LA01-01	1	
39	S-TAP SCREW 3X8	G614-300408-10A	4	
38	METAL PLATE FOR STAND SUPPORT PLATE	G423-27LA08-01	1	
37	ROHS S-TAP SCREW BID 3.0X8	G611-300408-10A	2	
36	STAND COVER	G230-26LA11-01R	1	
35	S-TAP SCREW 4X40	G614-400440-00A	2	
34	MECH SCREW M4X10	G604-407010-00A	2	
33	STAND SUPPORT PLATE	G423-27LA0A-01	1	
32	MECH SCREW M5X22	G604-500822-00A	4	
31	MECH SCREW M3X8	G604-305008-00A	3	
30				DISABLE
29	S-TAP SCREW 4X16	G614-400416-00A	14	
28	BACK CABINET BLACK LCT27AE WITH DVD	G202-L26AE01-01AAA	1	
27	S-TAP SCREW WHR 3X10	G612-300110-10A	8	
26	AC JACK BRACKET	G426-L37AD01-01SA	1	
25	POWER-CABLE	G774PL26AE01-01	1	
24	S-TAP SCREW 3X6	G614-300106-10A	2	
23	ROHS MECH SCREW BID M4X6	G600-407006-10A	4	
22	ROHS MECH SCREW CTS M3X6	G601-305006-10A	2	
21	BRACKET FOR VISA-MOUNT	G424-L26AD01-01SA	2	
20	SHIELD COVER FOR MAIN PCB	G483-L26AD11-01SA	1	
19	ROHS MECH SCREW PAN-WASHER M3X4	G602-305004-10A	9	
18	PCB-POWER	GE7801-P02001-2	1	
17	ROHS MECH SCREW PAN-WASHER M3X6	G602-305004-10A	11	
16	TERMINAL SHEET FOR MT5371 WITH DVD	G436-L26AD12-01SA	1	
15	MAIN PCB FOR MT5370	G771EL26AE03-01	1	
14	ROHS S-TAP,SCREW BID 4X10	G614-400412-10A	9	
13	ROHS MECH SCREW BID M4X6	G600-407006-10A	8	
12	PANEL BRACKET FOR V260B1-L01	G428-L26AD02-01SA	1	
11	ROHS S-TAP,SCREW BID 3X10	G614-300210-10A	6	
10	'Z'BRACKET FOR V260B1L01	G429-L26AD01-01SA	4	
9	DISPLAY LCT26' CMO V260B1_L01	CE6203-26CD01	1	
8	SPEAKER	G778-L26AE01-01	2	
7	REMOTE_PCB	G771BL26AE01-01	1	
6	REMOTE RECEIVE LENS	G269-42SD01-00LA	1	
5	S-TAP SCREW BID 3.0X8	G614-300108-10A	2	
4	S-TAP SCREW BID 2.6X8	G614-260208-10A	4	
3	KEY-PCB	G771KL26AE01-02	1	
2	FUNCTION KEY	G277-L37AE01-04ASA	1	
1	FRONT CABINET FOR LCT26AE	G200-L27AE02-00A	1	

DRAWN.					
CHECKED					
APPRD.					
3rd ANGLE PROJECTION					

TOLERENCE UNLESS OTHERWISE SPECIFIED	
0:	± 0.30
0.0:	± 0.10
0.00:	± 0.05
ANGULAR:	± 0.3°
UNIT : MM	

KAWA ELECTRONIC R & D CENTRE

MATL.

FINISH

TITLE EXPLODE VIEW FOR LCT26AE WITH DVD

MODEL NO. LCT26AE

A0	PART NO. EXP-L26AE01-01	DWG. NO. L26AEEXP1
SCALE	QTY.	SHEET OF

Spare part list for LCT26Z4AD

Item	Part Number	Part Description	Usage / unit	Unit	Key/Spare
	GLCT26AEADA1CS-B01	ROHS AKAI LCT26AE (LCT26Z4AD) S-MT5370+DVD CMO(V260B1-L01) AC120V/60HZ USA BLACK/ SILVER ATV/DTV			
1>	G510-L26AE02-01AKA	ROHS CARTON BOX V LCT26Z4AD AKAI DONG XING	1.000000	Piece	K
2>	G580-K00201-05APA	ROHS IB E FOR AKAI W/DVD K002(OMNIPOTENCE) REMOTE CONTROL USA(CHENG YI)	1.000000	Piece	K
3>	G580-L26AE1A-01APA	ROHS IB E FOR AKAI LCT26Z4AD TV+DTV+DVD NO PIP CMO MT5370 USA(RS) (CHENG YI)	1.000000	Piece	K
4>	GE7501-063014A	ROHS REMOTE CONTROL AKAI K002 COMBO 60KEYS BLACK SET CODE218 (CHUAN QI SHENG)	1.000000	SET	K
5>	GE7801-P02001-2	ROHS PCB ASSY PSU BOARD MEGMEET MLT168K FOR 26&27LCD AC110-240V OUTPUT 12V/9V/24V/5V 200W	1.000000	SET	K
6>	G771EL26AE03-01	ROHS MAIN ASS'Y S-MT5370 +DVD CMO USA	1.000000	SET	K
7>	G200-L27AE02-01AAA	ROHS CABINET FRONT LCT26AE SILVER/BLACK(P320-605871K-00)(AKAI PLASTIC)	1.000000	Piece	S
8>	G202-L26AE01-01AAA	ROHS CABINET BACK LCT26AE W/DVD BLACK(AKAI PLASTIC)	1.000000	Piece	S
9>	G258-L27AD21-01RA	ROHS DVD FUNCTION KNOB COVER KNOB BLACK R(AKAI PLASTIC)	1.000000	Piece	S
10>	G269-42SD01-01LA	ROHS REMOTE RECEIVE LENS (AKAI PLASTIC)	1.000000	Piece	S
11>	G277-L27AD11-01SA	ROHS DVD FUNCTION KNOB BLK LCT2701TD S(AKAI PLASTIC)	1.000000	Piece	S
12>	G277-L37AE01-04ASA	ROHS FUNCTION KNOB MATT BLACK(P320-605871K-00) S (AKAI PLASTIC)	1.000000	Piece	S
13>	G300-L26AE01-02CA	ROHS POLYFORM BOTTOM FOR LCT26AE VERTICAL CHUANG YI	1.000000	Piece	S
14>	G300-L26AE02-02CA	ROHS POLYFORM TOP FOR LCT26AE VERTICAL CHUANG YI	1.000000	Piece	S
15>	G310-030404-05VA	ROHS POLYBAG FOR SCREW 3"X4"X0.04MM(AO LANG)	1.000000	Piece	S
16>	G310-041204-01VA	ROHS POLYBAG 4"X12"X0.04 AV(AO LANG)	1.000000	Piece	S

17>	G310-111404-05VA	ROHS POLYBAG 11"X14"X0.04MM (AO LANG)	1.000000	Piece	S
18>	G310-383550-07VA	ROHS POLYBAG LAMIFILM 38"X35"X0.5MM AO LANG	1.000000	Piece	S
19>	G424-L26AD01-01SA	ROHS BRACKET FOR VISA-MOUNT(TOMEI)	2.000000	Piece	S
20>	G426-L37AD01-01SA	ROHS AC LINE BRACKET (TOMEI)	1.000000	Piece	S
21>	G428-L26AD02-01SA	ROHS PANEL BRACKET FOR V260B1-L01(5370) (NEW BA-CAB)(TOMEI)	1.000000	Piece	S
22>	G436-L26AD12-01SA	ROHS TERMINAL SHEET FOR MT5370 WITH DVD LCT26AD (TOMEI)	1.000000	Piece	S
23>	G481-L26AD01-01SA	ROHS BRACKET FOR DVD NEON(TOMEI)	1.000000	Piece	S
24>	G483-L26AD11-01SA	ROHS SHIELD COVER FOR MAIN PCB TINPLATE T=0.3 (TOMEI)	1.000000	Piece	S
25>	G522-421D01-01A	ROHS MASKING PAPER (ZHI QIANG SHENG)	1.000000	Piece	S
26>	G530-080032-10A	ROHS FBP WHR 3.2X8.0X1.0 (ZHI QIANG SHENG)	1.000000	Piece	S
27>	G560-L26AE01-02APA	ROHS MODEL LABEL AKAI LCT26Z4AD A(QIAN SE)	1.000000	Piece	S
28>	G563-119-A	ROHS SERIAL NO. LABEL	1.000000	Piece	S
29>	G568-P46T02-02A	ROHS WARNING LB ENG 42SF NIL	1.000000	Piece	S
30>	G578-L26AE01-01APA	ROHS FUNCTION SHEET LABEL FOR MT5370 TWO HDMI W/DVD P(QIAN SE)	1.000000	Piece	S
31>	G579-42D102-09A	ROHS SERIAL NO/BAR CODE LABEL 42D1	1.000000	Piece	S
32>	G579-42D105-01A	ROHS PROTECTIVE EARTH LABEL FOR ESA 42TD1	1.000000	Piece	S
33>	G579-L26AE01-02APA	ROHS UPC LABEL LCT26Z4AD UPC NO: 827935512688(QIAN SE)	2.000000	Piece	S
34>	G579-L26AE02-01APA	ROHS PDP LABEL ONE AKAI LCT26Z4AD(QIAN SE)	1.000000	Piece	S
35>	G579-L26AE03-01APA	ROHS PDP LABEL TWO AKAI LCT26Z4AD(QIAN SE)	1.000000	Piece	S

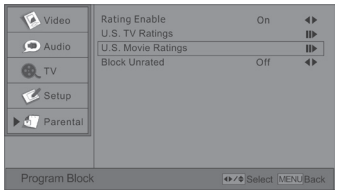
36>	G579-L27AD09-01A	ROHS CAUTION LABEL ENG AKAI (QIAN SE)	1.000000	Piece	S
37>	G579-L32AD03-02A	ROHS CLASS I LASER PRODUCT LOGO(QIAN SE)	1.000000	Piece	S
38>	G579-L32AD09-02APA	ROHS FCC STATEMENT LABEL 77X20MM(QIAN SE)	1.000000	Piece	S
39>	G590-L26AE01-02APA	ROHS WARRANTY CARD LCT26Z4AD W/DVD P(QIAN SE)	1.000000	Piece	S
40>	G593-L26AE01-02APA	ROHS QUICK START GUIDE LCT26Z4AD W/DVD P(QIAN SE)	1.000000	Piece	S
41>	G614-300106-10A	ROHS S-TAP SCREW BID 3.0X6 (HUA CHUANG)	2.000000	Piece	S
42>	GE3404-157013A	ROHS AC CORD UL 1.88M FOR MT8202 (W/HOUSING) (YUN HUAN)	1.000000	Piece	S
43>	GE3421-925240A	ROHS WIRE ASSY 1H2.5-2H2.5 L=400 AG 8P/4+10P LCT27&32" MT5371 (HU GUANG)	1.000000	Piece	S
44>	GE3421-925242A	ROHS WIRE ASSY 1H2.5-2H2.5 L=400 AG 12P/7+11P LCT27&32" MT5371 (HU GUANG)	1.000000	Piece	S
45>	GE3461-000140A	ROHS WIRE ASSY 1H2.0-2H2.5/2.0 L700/450 14P/8P+4P (HU GUANG)	1.000000	Piece	S
46>	GE3471-000048A	ROHS WIRE WS SHIELD WIRE FOR 32LCD TV+COMBO KEY WIRE FOR DVD (HU GUANG)	1.000000	Piece	S
47>	GE3471-000097A	ROHS WIRE ASSY 1H2.0-2H2.0 L=410 DJ/DV 11/12P MT5371 COMBO (HU GUANG)	1.000000	Piece	S
48>	GE3471-000103A	ROHS WIRE WS 1H2.0-2H2.0 L=550 DI 13P/6+8P LCT27&42" MT5371 KEY (HU GUANG)	1.000000	Piece	S
49>	GE3471-000125A	ROHS WIRE WS 1H1.25-2H1.0 L200 DD 30P LCT26" MT5371 LVDS (HU GUANG)	1.000000	Piece	S
50>	GE3471-000142A	ROHS WIRE ASSY 1H2.0-2H2.0 10P/6P+5+2P L500 (HU GUANG)	1.000000	Piece	S
51>	GE4801-124001A	ROHS SPEAKER 8 OHM 10W D3" YD78-1(JUN LANG)	2.000000	Piece	S
52>	GE6203-26CD01	ROHS DISPLAY LCD26" CMO V260B1-L01 REV:B2 1366X768 800:1	1.000000	Piece	S
53>	GE7301-010002A	ROHS BATTERY AAA R03P1.5V <2> (CHAO YANG)	2.000000	Piece	S
54>	GE7801-D02002	ROHS DVD PCB ASSY LITAI FOR MT8202&MT5371 USA (LI TAI)	1.000000	SET	S

55>	G734-L27AD03-03	ROHS ELLIPSE PLASTIC BASE ASS'Y ROUND W/O PACKING BLACK(P320-605871K-00)	1.000000	SET	S
56>	G771BL26AE01-01	ROHS IR RECEIVE PCB ASS'Y S-MT5370+DVD CMO	1.000000	SET	S
57>	G771KL26AE01-01	ROHS KEY (DVD 3KEYS) PCB ASS'Y S-MT5370+DVD CMO	1.000000	SET	S
58>	G771KL26AE01-02	ROHS KEY (MAIN 7KEYS)PCB ASS'Y S-MT5370+DVD CMO	1.000000	SET	S

If you forget your V-Chip Password:

◆ Using the “U.S. Movie Ratings” item

1. After entering the “Program Block” menu, press ▲ or ▼ button to highlight the “U.S. Movie Ratings” item.
2. Press ► or **Enter** button to enter.
3. Press ▲ or ▼ button to select an item, then press the **Enter** button to lock (display “🔒”) or unlock (display “☐ ”).



For Movie previously shown in theaters:

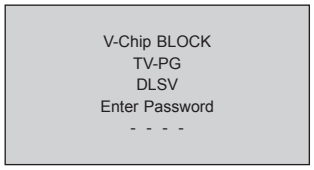
- G (general audience)
- PG (parental guidance suggested)
- PG-13 (13 years and older)
- R (Restricted)
- NC-17 (18 years and older)
- X (Adult)

If you set PG-13: G and PG movies be available, PG-13, R, NC-17, and X will be blocked.

4. Press the **Menu** button to exit the sub-menu.

◉ Unlocking programs temporarily

1. If you try to watch a program that exceeds the TV Guideline you set, the system enters program lock mode. You can either unlock the program temporarily or select a non-locked program to watch.



2. To temporarily unlock the program, press the Number buttons (0~9) to enter your 4-digit password.

If the correct code is entered, the program lock mode is released and the normal picture appears.

Software Upgrade

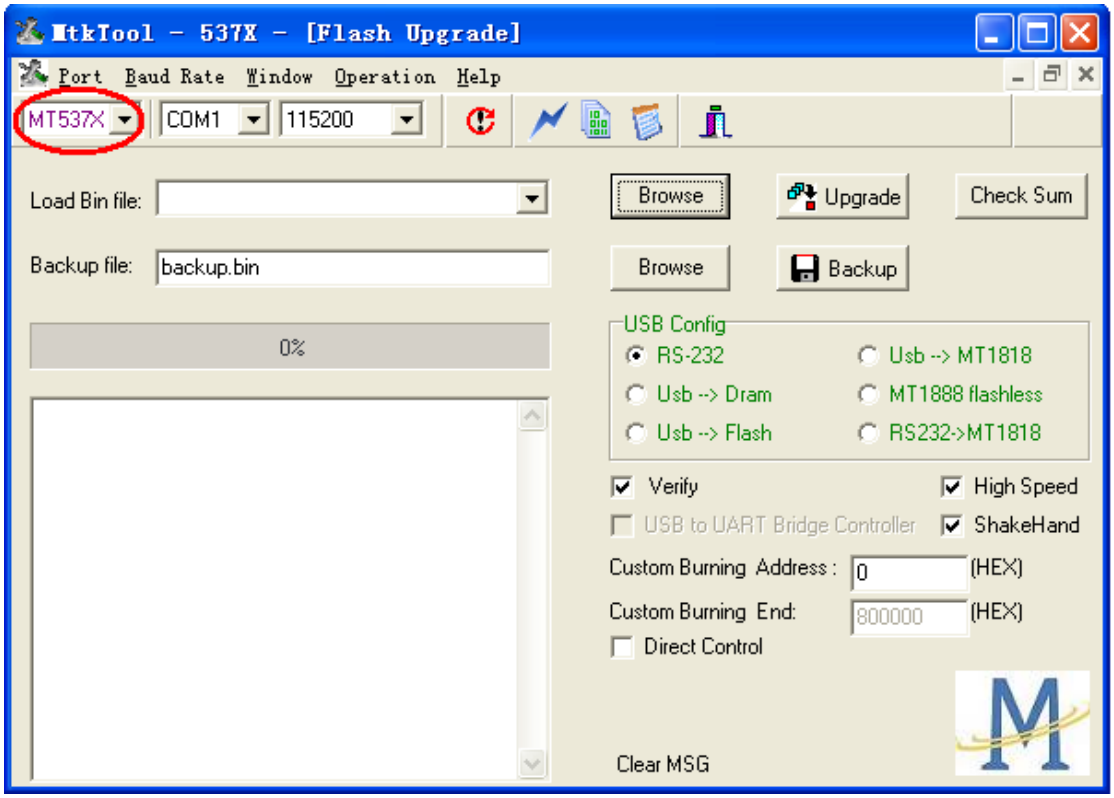
Process of update MT537X

Preparing :

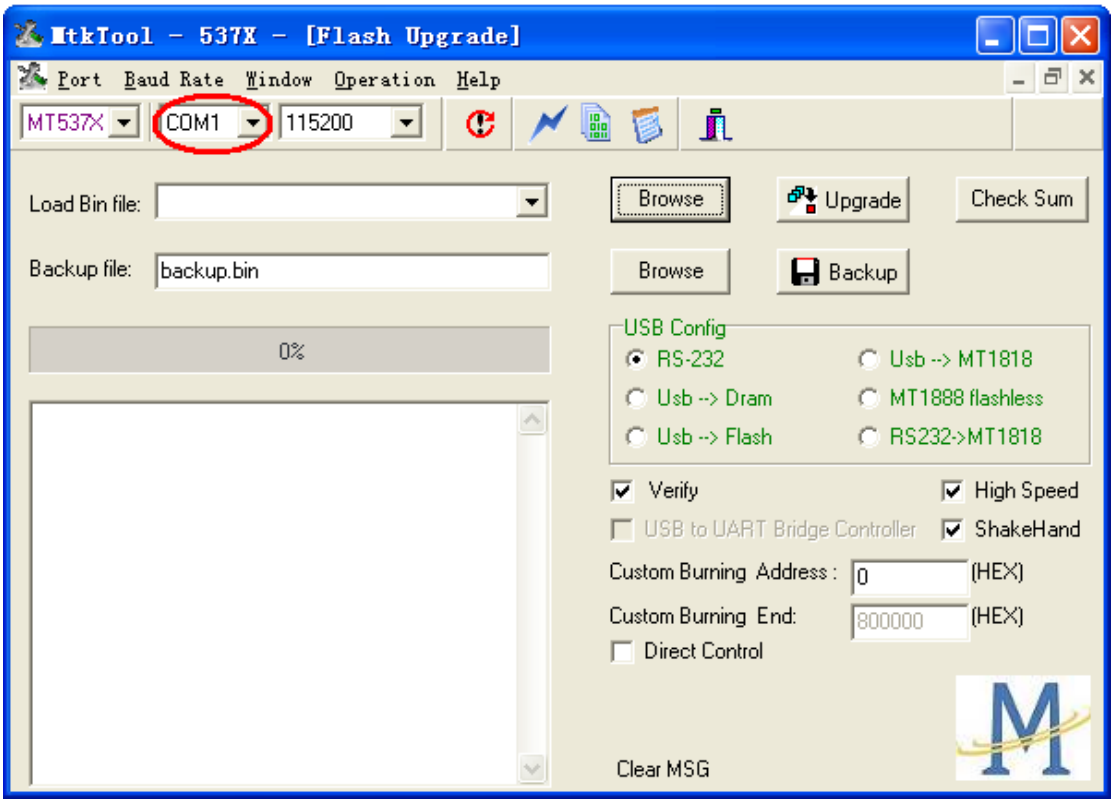
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**.Please find the details for connecting **refering to the appendix at the end of this file.**
2. Store the MtkTool into the PC .

Downloading :

3. Turn on AC power of the TV and then press the button “standby” of the remote control . The image could be found on the screen of the TV while the color of the power indicator is green .
4. Execute MTKtool and select the chipset as MT537X. (the software of MTKtool will be sent to your side)

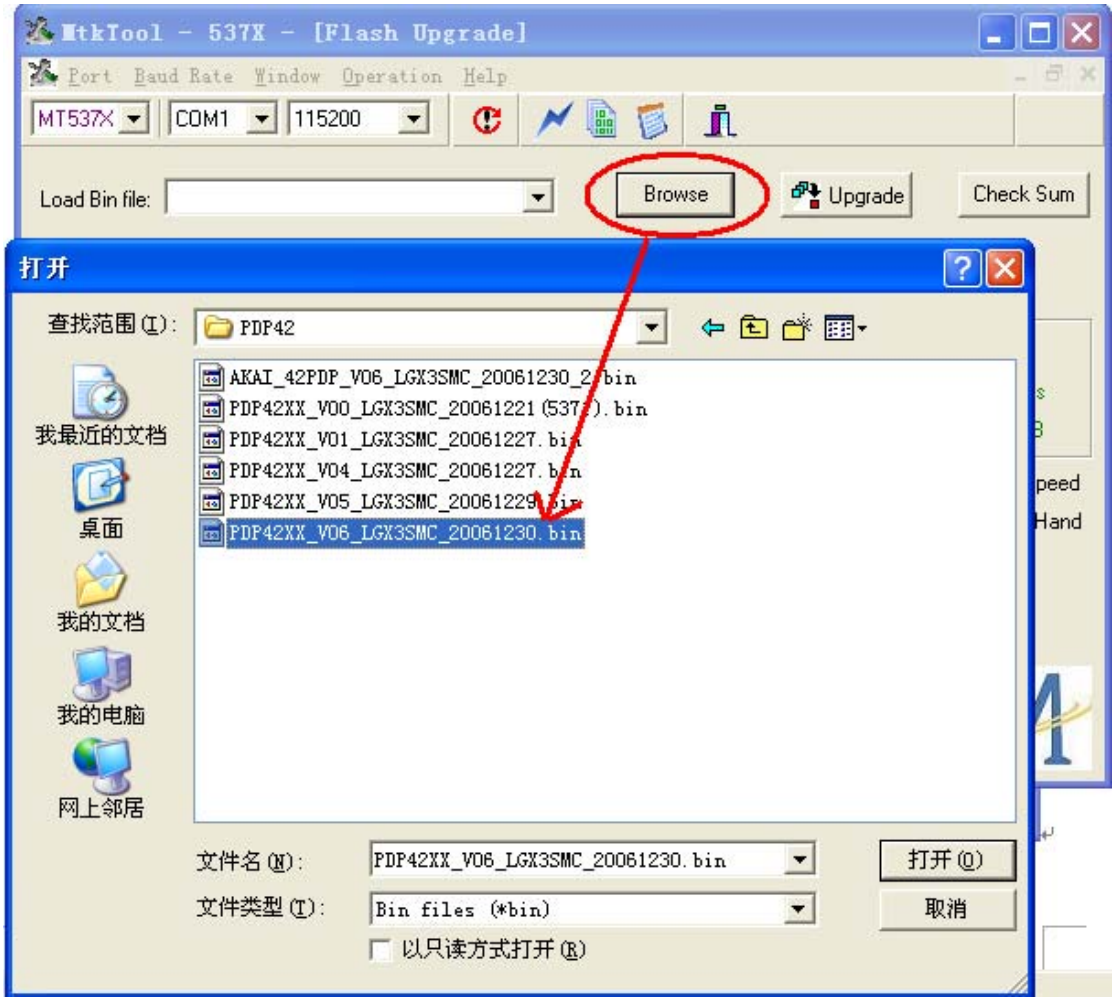


5. Select current COM port. (please try to check the COM port of your PC).

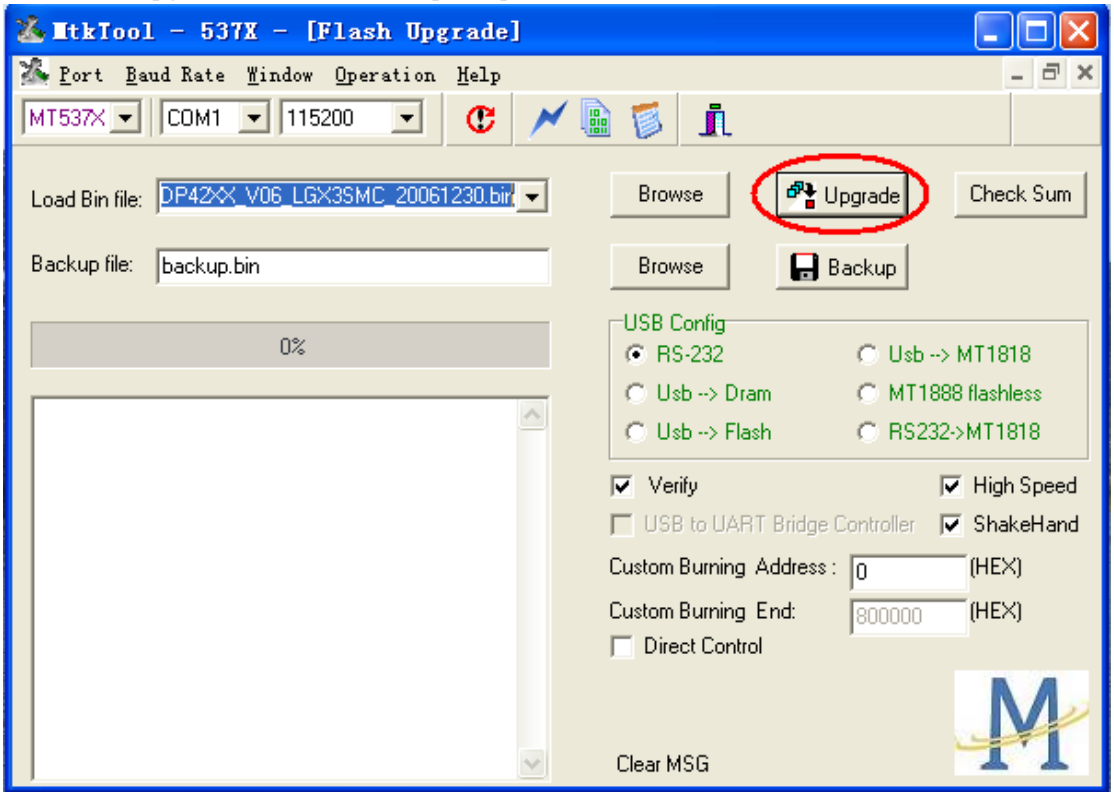


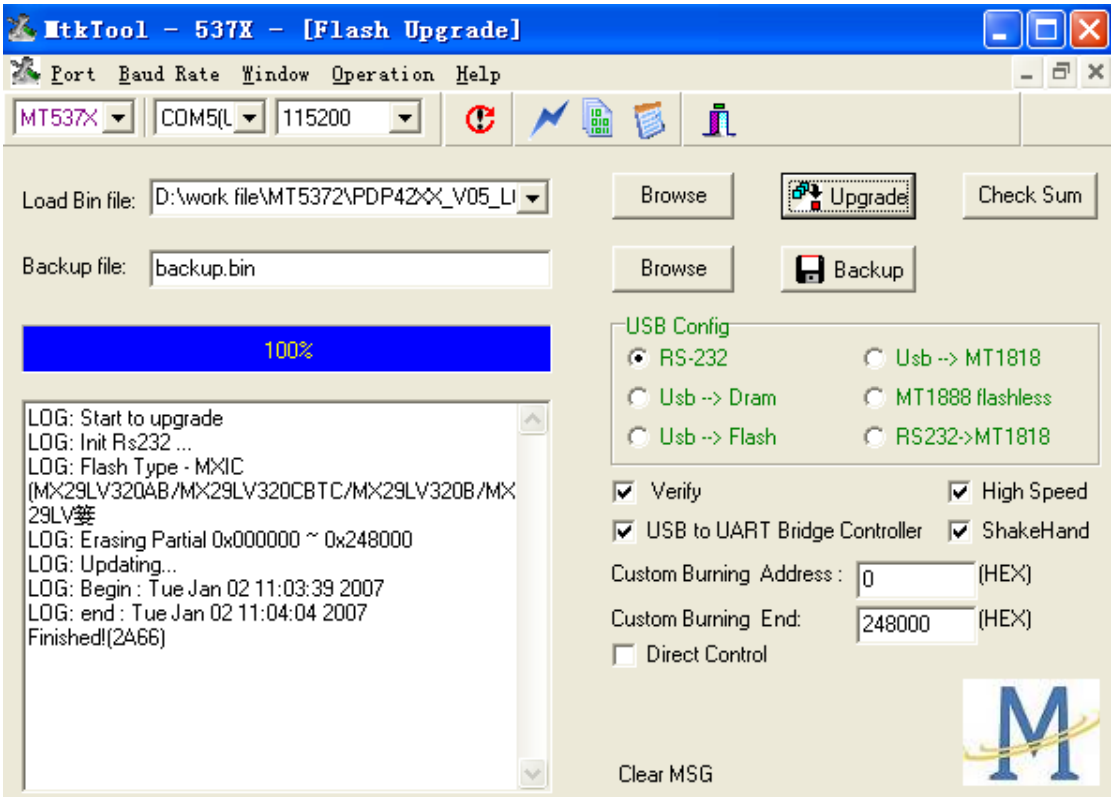
6. Choose the bit rate as 115200.

7. Select the update binary by pressing browse button. For example,the binary file name is PDP42XX_V06_LGX3SMC_20061230.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.





9. The update process is successful as the progress bar is 100%. After the update process is ok, turn off power and wait indicator light is off. Turn on power and TV can work.

Checking

It is needed to check the version of the firmware for MT5371 which has been download into the TV .

Press Menu button of the remote control，following input “5371”of the remote control and OSD menu for Factory Setting is appeared on the screen .

Use the remote control and select the item of “Version Info” and then press “Enter” button of the remote control. It is easy to be found the version of the current firmware for MT5371 is as the following : “Model Name : PDP42Z5TA
/ Version:V17_LGX3SMC_20070119 ”

Appendix:

Quick Installation Guide

For

Software Upgrade Board

1. Parts List

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 – VGA cable (#4)
- USB cable x 1 (#5)

2. Installation for ATV upgrade

2.1 Connect RS232 cable (#2) to PC serial port

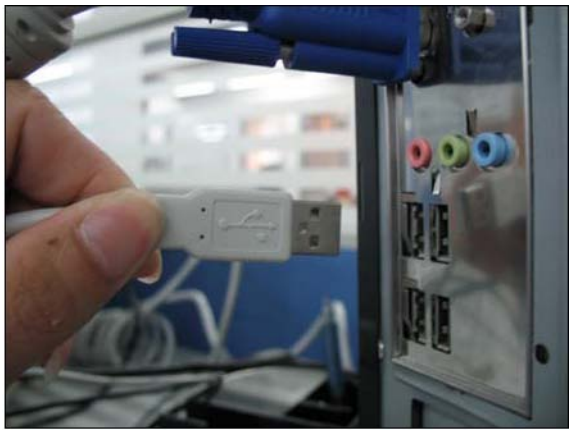
Connect another side of RS232 cable (#2) to the board (#1)

2.2 Connect RS232-VGA cable (#4) (RS232 side) to the board (#1)

Connect RS232-VGA cable (#4) (VGA side) to the TV

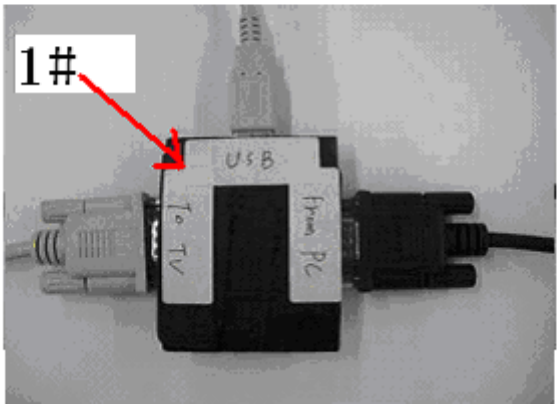
2.3 Connect USB cable (#5) to the board (#1)

Connect another side of USB cable (#5) to PC

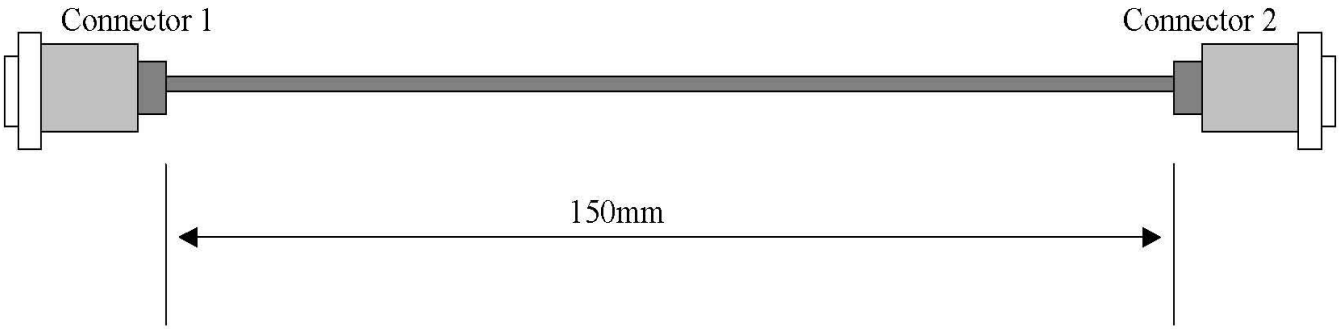


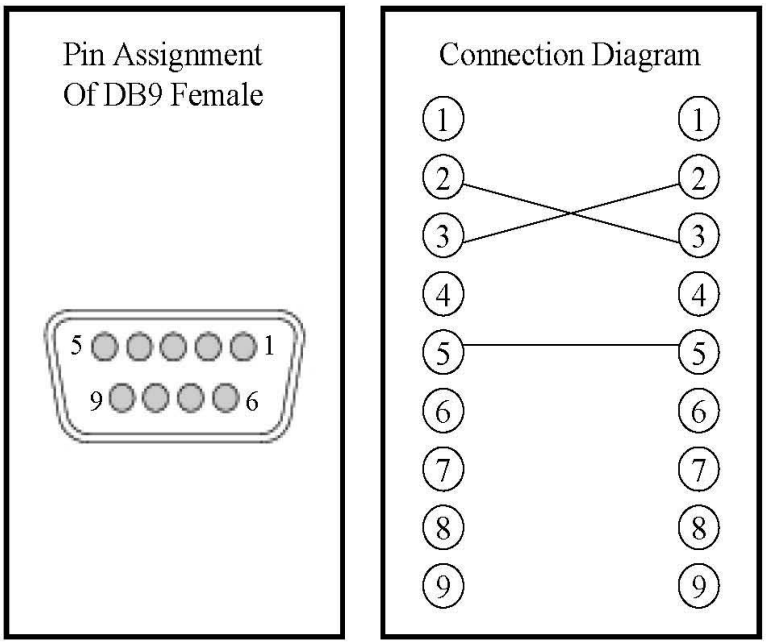
3. Cables Standard for Upgrade Board

Software upgrade board x 1 (#1)



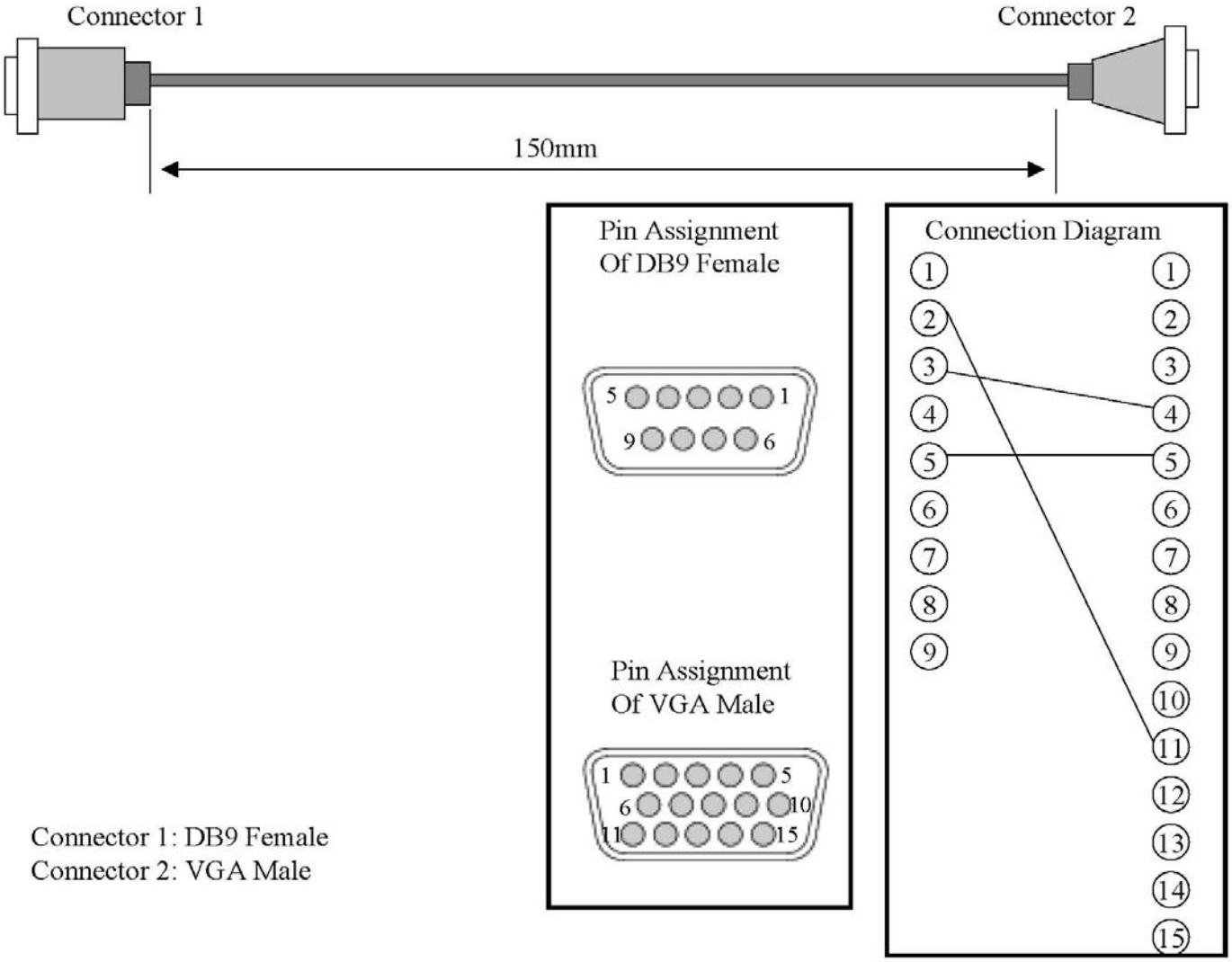
RS232 Null Cable for PC (#2)





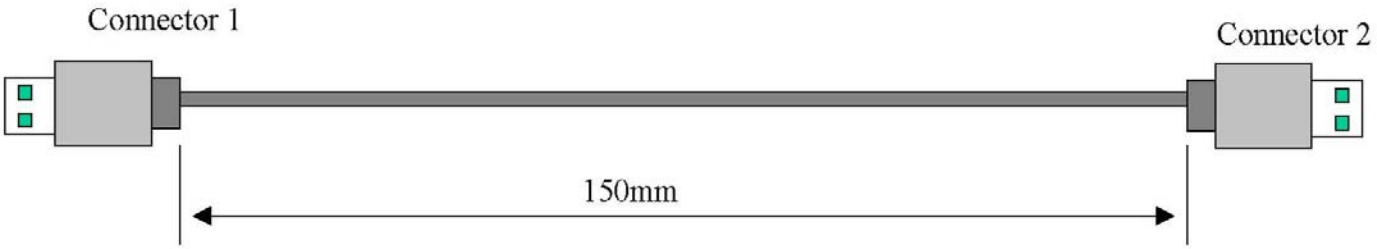
Connector 1: DB9 Female
Connector 2: DB9 Female

RS232 - VGA Cable (#4)



Connector 1: DB9 Female
Connector 2: VGA Male

USB Cable (#5)



Connector 1: Standard USB Male
Connector 2: Standard USB Male